ATTENTION
OBSERVE PRECAUTIONS
FOR HANDLING
ELETROSTATIC
SENSITIVE
DEVICES

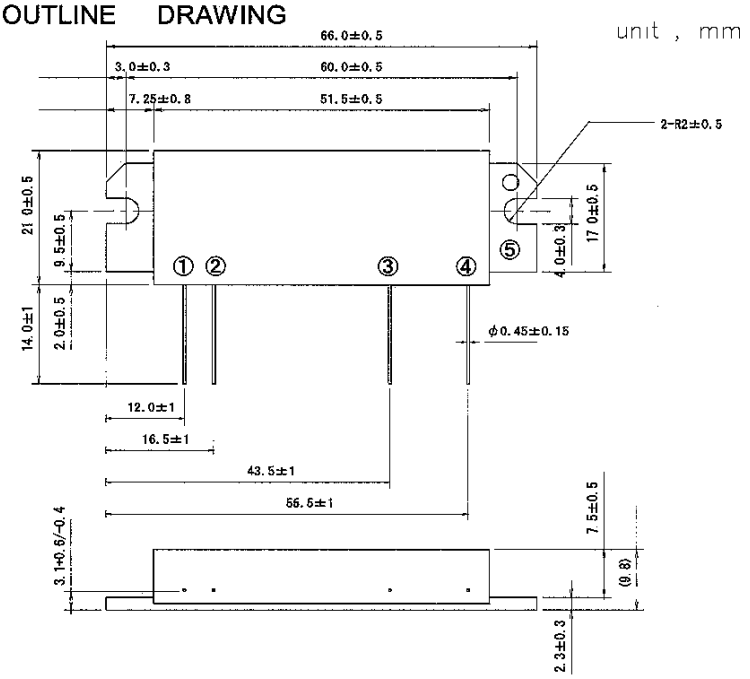
Revision date: 1st/Feb. '02

MITSUBISHI RF POWER MODULE

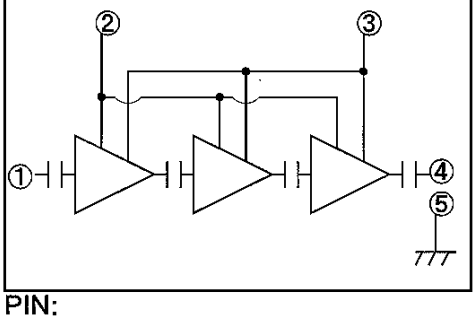
RA30H3340M

Silicon MOS FET Power Amplifier, 330-400MHz 30W MOBILE RADIO

OUTLINE DRAWING



BLOCK DIAGRAM



PIN:
1 Pin :RF INPUT
2 VGG:GATE BIAS SUPPLY
3 VDD:DRAIN BIAS SUPPLY
4 Po :RF OUTPUT
5 GND:FIN

MAXIMUM RATINGS (Tc=25deg.C UNLESS OTHERWISE NOTED)

SYMBOL	PARAMETER	CONDITIONS	RATINGS	UNIT
VDD	SUPPLY VOLTAGE	VGG<5V,Zg=Zl=50ohm	17	V
VGG	GATE BIAS VOLTAGE	VDD<12.5V,Pin=0mW,Zg=Zl=50ohm	6	V
Pin	INPUT POWER	f=330-400MHz,Zg=Zl=50ohm	100	mW
Po	OUTPUT POWER	f=330-400MHz,Zg=Zl=50ohm	45	W
Tc(OP)	OPERATION CASE TEMPERATURE	f=330-400MHz,Zg=Zl=50ohm	-30 to +110	deg.C
Tstg	STORAGE TEMPERATURE		-40 to +110	deg.C

Note:Above parameters are guaranteed independently.

ELECTRICAL CHARACTERISTICS (Tc=25deg.C,Zg=Zl=50ohm UNLESS OTHERWISE NOTED)

SYMBOL	PARAMETER	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
f	FREQUENCY RANGE		330		400	MHz
Po	OUTPUT POWER	Vdd=12.5V,Vgg=5V,Pin=50mW	30			W
Et	TOTAL EFFICIENCY		40			%
2fo	2nd HARMONIC				-25	dBc
VSWR in	INPUT VSWR				3:1	-
	Stability	Zg=50ohm, Vdd=10 - 15.2V, LOAD VSWR = 3:1, Pin=25 - 70mW, Po<40W(Vgg Control)	No parasitic oscillation			
	LOAD VSWR TOLERANCE	Vdd=15.2V, Pin=50mW, Po=30W(Vgg Control), Zg=50ohm, LOAD VSWR = 20:1	No degradation or destroy			-

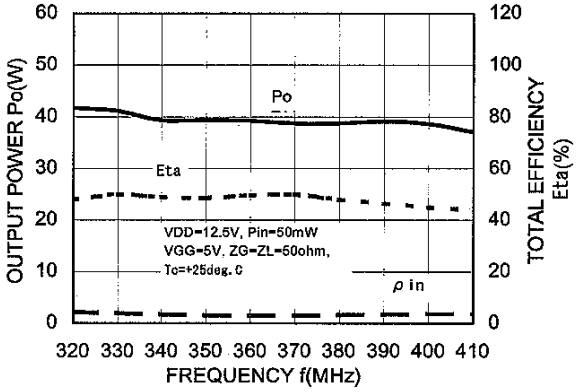
ABOVE PARAMETERS, RATINGS, LIMITS AND CONDITIONS ARE SUBJECT TO CHANGE .

Keep safety first in your circuit designs!

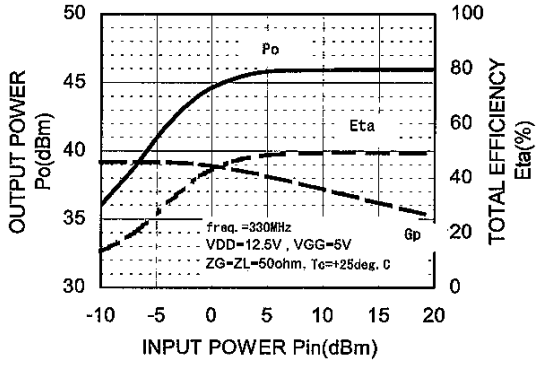
Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

TYPICAL PERFORMANCE DATA

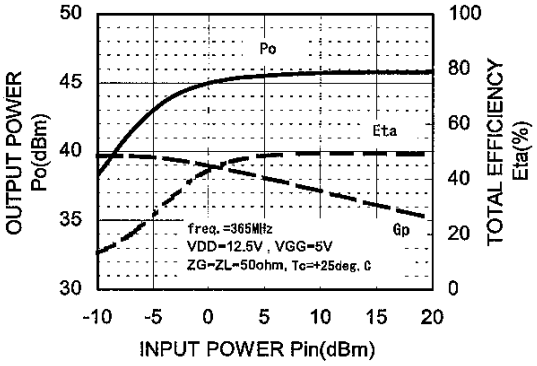
OUTPUT POWER, TOTAL EFFICIENCY, INPUT VSWR VS. FREQUENCY



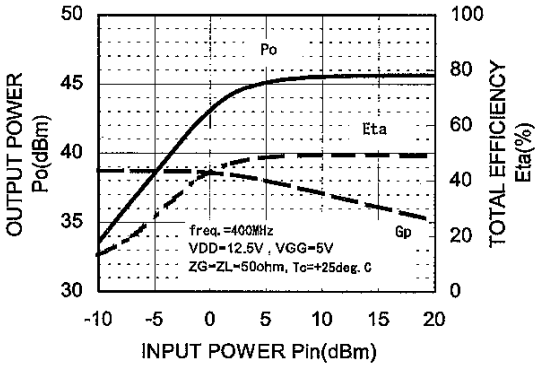
OUTPUT POWER, EFFICIENCY VS. INPUT POWER



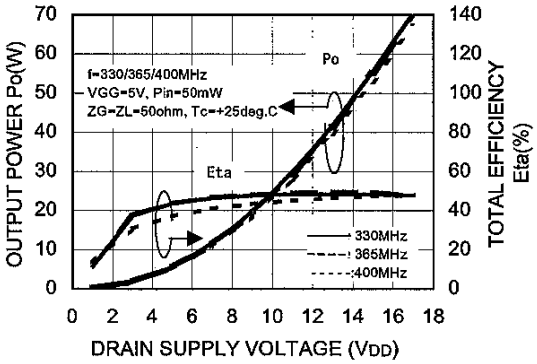
OUTPUT POWER, EFFICIENCY VS. INPUT POWER



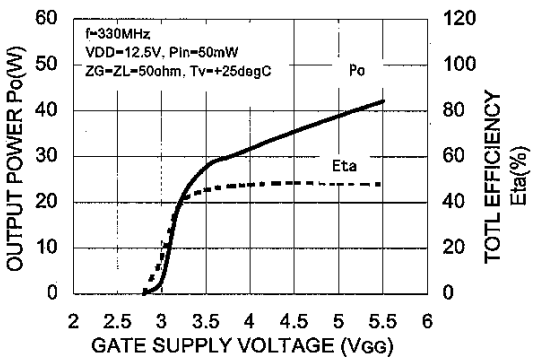
OUTPUT POWER, EFFICIENCY VS. INPUT POWER



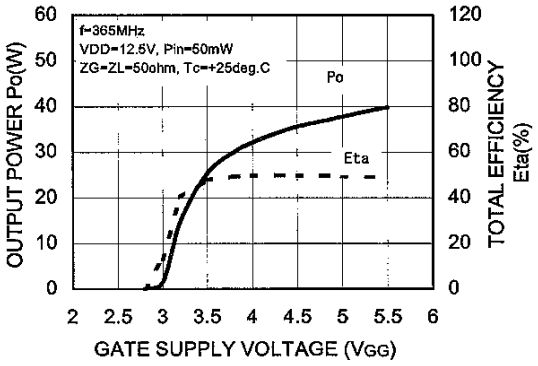
OUTPUT POWER, EFFICIENCY VS. DRAIN SUPPLY VOLTAGE



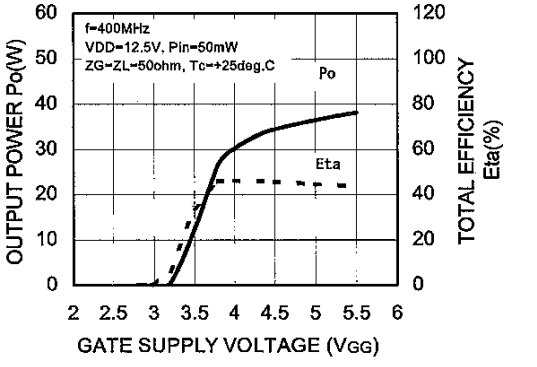
OUTPUT POWER, EFFICIENCY VS. GATE SUPPLY VOLTAGE



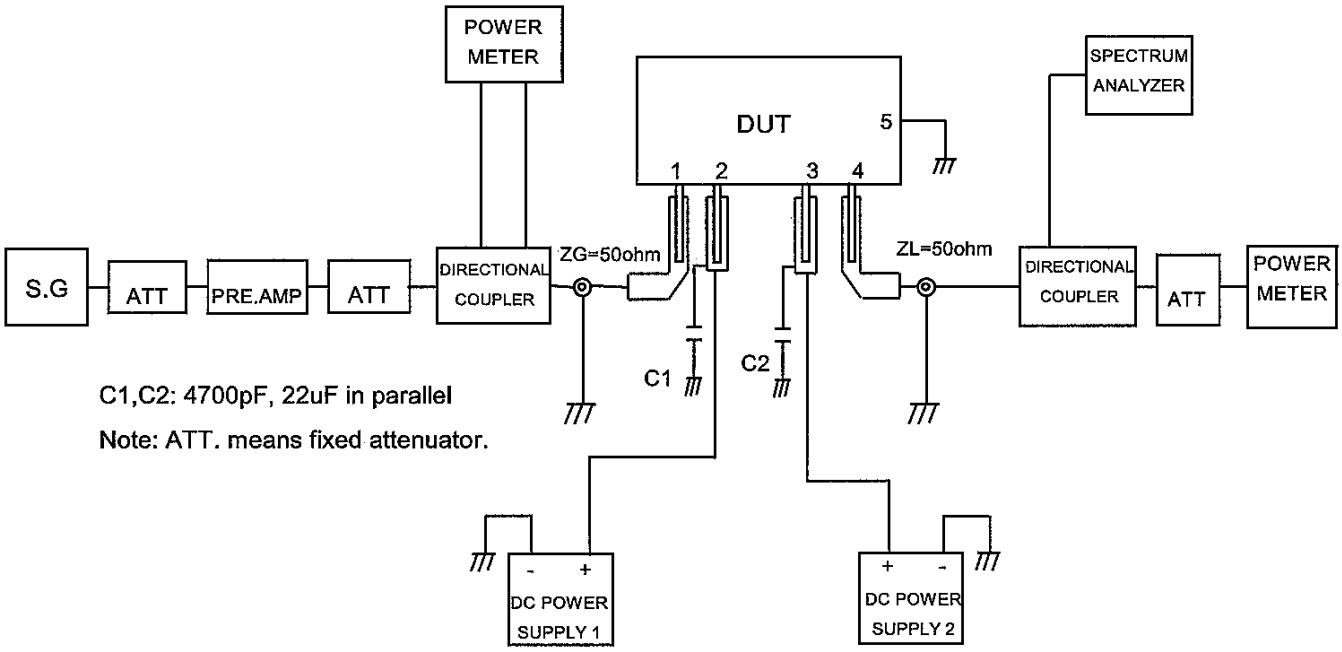
OUTPUT POWER, EFFICIENCY VS. GATE SUPPLY VOLTAGE



OUTPUT POWER, EFFICIENCY VS. GATE SUPPLY VOLTAGE



TEST BLOCK DIAGRAM



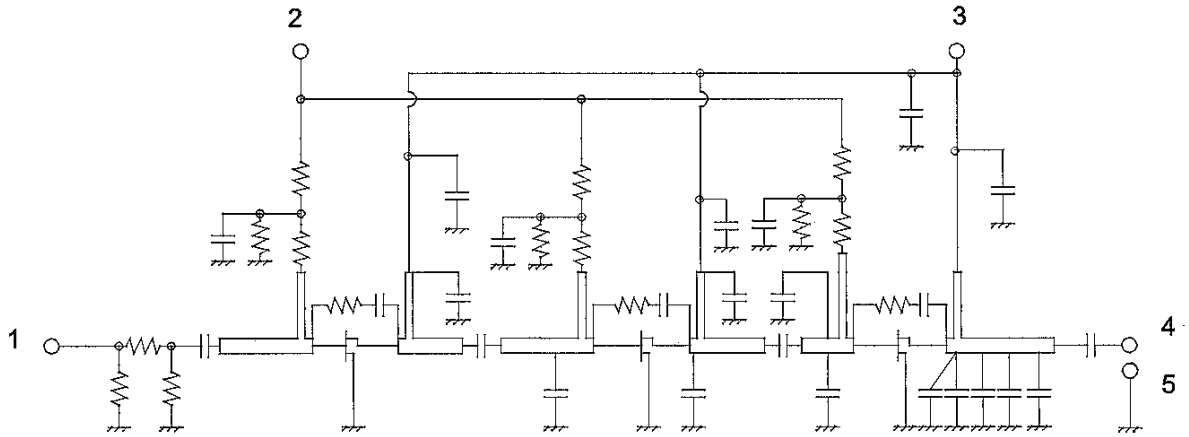
C1,C2: 4700pF, 22uF in parallel

Note: ATT. means fixed attenuator.

PINING

1. Input terminal
2. Vgg bias terminal
3. Vdd bias terminal
4. Output terminal
5. Ground (FIN)

EQUIVALENT CIRCUIT



RA30H3340M DESIGN CONSIDERATION OF HEAT RADIATION

A. Junction temperature

The condition at standard operation for each stage transistors are shown in Table 1.

Standard operation :

Pout = 30W, Vcc = 12.5V, Pin = 50mW,

Eta = 40 %(min. rate)

Table 1.

Stage	Vdd(V)	Idd(A)	Pin(W)	Pout(W)	Rth(j-c) (deg.C/W)
1st	12.5	0.30	0.05	1.5	5.0
2nd	12.5	1.50	1.5	9.0	2.4
Final	12.5	4.20	9.0	30.0	1.2

(1) Junction temperature of the 1st stage transistor

Tj1 = (Vdd x Idd1 - Pout1 + Pin1) x Rth1(j-c) + T(case)

= (12.5 x 0.30 - 1.5 + 0.05) x 5.0 + T(case)

11.5 + T(case) (deg.C)

(2) Junction temperature of the 2nd stage transistor

Tj2 = (Vdd x Idd2 - Pout2 + Pin2)x Rth2(j-c) + T(case)

= (12.5 x 1.5 - 9 + 1.5) x 2.4 + T(case)

= 27.0 + T(case) (deg.C)

(3) Junction temperature of the Final stage transistor

Tj3 = (Vdd x Idd3 - Pout3 + Pin3)x Rth3(j-c) + T(case)

= (12.5 x 4.2 - 30.0 + 9.0) x 1.2 + T(case)

= 37.8 + T(case) (deg.C)

B. Heat sink design

In thermal design of heat sink, keep the case temperature below 90 deg.C at Pout = 30W standard operation and ambient temperature 60 deg.C.

The thermal resistance Rth (case - air) of the heat sink to realize this :

Rth (case - air) = (Tcase - Tair) / ((Pout / Eta) - Pout + Pin)

= (90 - 60) / ((30 /0.40) - 30 +0.05)

= 0.67 (deg.C / W)

Note : Including the contact thermal resistance between device and heat sink.

Mounting the device on the heat sink with above thermal resistance, junction temperatures of each transistors become :

Tj1 = 101.5 (deg.C)

Tj2 = 117.0 (deg.C)

Tj3 = 127.8 (deg.C)

at T(air) = 60 deg.C , T(case) = 90 deg.C

Since the annual average of ambient temperature is 30 deg.C, junction temperature of each transistors become :

Tj1 = 71.5 (deg.C)

Tj2 = 87.0 (deg.C)

Tj3 = 97.8 (deg.C)

As the maximum junction temperature of these incorporated transistors Tjmax are 175 deg.C, application under debated conditions is ensured.