TDA5051A

Home automation modem

Rev. 5 — 13 January 2011 Product data sheet

1. General description

The TDA5051A is a modem IC, specifically dedicated to ASK transmission by means of the home power supply network, at 600 baud or 1200 baud data rate. It operates from a single 5 V supply.

2. Features and benefits

- Full digital carrier generation and shaping
- Modulation/demodulation frequency set by clock adjustment, from microcontroller or on-chip oscillator
- High clock rate of 6-bit D/A (Digital to Analog) converter for rejection of aliasing components
- Fully integrated output power stage with overload protection
- Automatic Gain Control (AGC) at receiver input
- 8-bit A/D (Analog to Digital) converter and narrow digital filtering
- Digital demodulation delivering baseband data
- Easy compliance with EN50065-1 with simple coupling network
- Few external components for low cost applications
- SO16 plastic package

3. Applications

- Home appliance control (air conditioning, shutters, lighting, alarms and so on)
- Energy/heating control
- Amplitude Shift Keying (ASK) data transmission using the home power network

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	supply voltage			4.75	5.0	5.25	V
$I_{DD(tot)}$	total supply current	f_{osc} = 8.48 MHz					
		Reception mode		-	28	38	mA
		Transmission mode; $\overline{DATA\_IN}$ = 0; Z_L = 30 Ω	[1]	-	47	68	mA
		Power-down mode		-	19	25	mA
f_{cr}	carrier frequency		[2]	-	132.5	-	kHz
f_{osc}	oscillator frequency			6.08	-	9.504	MHz
$V_{o(rms)}$	output carrier signal (RMS value)	$\overline{DATA\_IN}$ = LOW; Z_L = CISPR16		120	-	122	dBμV
$V_{i(rms)}$	input signal (RMS value)		[3]	82	-	122	dBμV
THD	total harmonic distortion on CISPR16 load with coupling network			-	–55	-	dB
T_{amb}	ambient temperature			–50	-	+100	°C

[1] The value of the total transmission mode current is the sum of $I_{DD(RX/TX)(tot)}$ + $I_{DD(PAMP)}$ in the Table 5 “Characteristics”.

[2] Frequency range corresponding to the EN50065-1 band. However, the modem can operate at any lower oscillator frequency.

[3] The minimum value can be improved by using an external amplifier; see application diagrams Figure 19 and Figure 20.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA5051AT	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

6. Block diagram

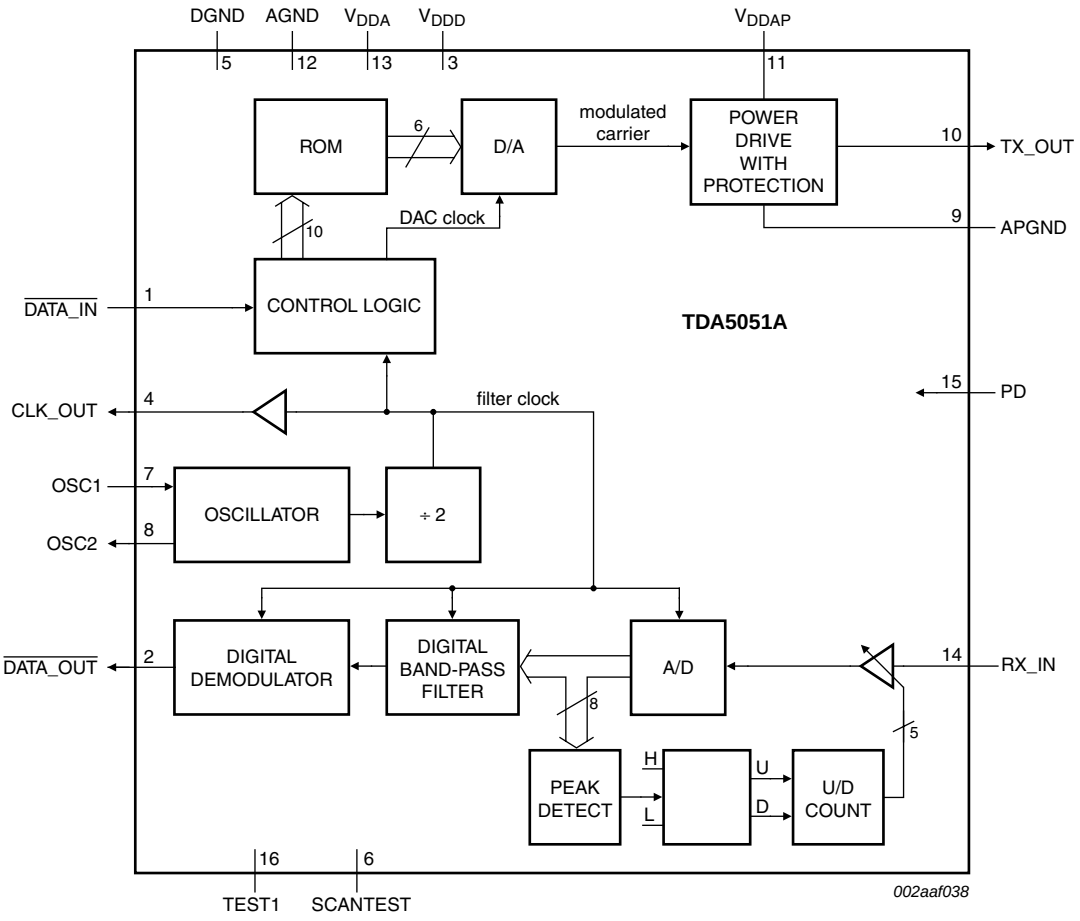


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

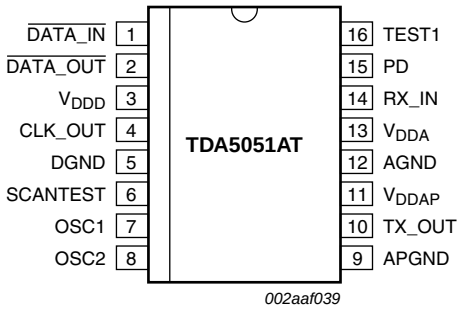


Fig 2. Pin configuration for SO16

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
$\overline{\text{DATA\_IN}}$	1	digital data input (active LOW)
$\overline{\text{DATA\_OUT}}$	2	digital data output (active LOW)
V_{DDD}	3	digital supply voltage
CLK_OUT	4	clock output
DGND	5	digital ground
SCANTEST	6	test input (LOW in application)
OSC1	7	oscillator input
OSC2	8	oscillator output
APGND	9	analog ground for power amplifier
TX_OUT	10	analog signal output
V_{DDAP}	11	analog supply voltage for power amplifier
AGND	12	analog ground
V_{DDA}	13	analog supply voltage
RX_IN	14	analog signal input
PD	15	power-down input (active HIGH)
TEST1	16	test input (HIGH in application)

8. Functional description

Both transmission and reception stages are controlled either by the master clock of the microcontroller or by the on-chip reference oscillator connected to a crystal. This ensures the accuracy of the transmission carrier and the exact trimming of the digital filter, thus making the performance totally independent of application disturbances such as component spread, temperature, supply drift and so on.

The interface with the power network is made by means of an LC network (see Figure 15). The device includes a power output stage that feeds a 120 dBμV (RMS) signal on a typical 30 Ω load.

To reduce power consumption, the IC is disabled by a power-down input (pin PD): in this mode, the on-chip oscillator remains active and the clock continues to be supplied at pin CLK_OUT. For low-power operation in reception mode, this pin can be dynamically controlled by the microcontroller, see Section 8.4 “Power-down mode”.

When the circuit is connected to an external clock generator (see Figure 6), the clock signal must be applied at pin OSC1 (pin 7); OSC2 (pin 8) must be left open-circuit. Figure 7 shows the use of the on-chip clock circuit.

All logic inputs and outputs are compatible with TTL/CMOS levels, providing an easy connection to a standard microcontroller I/O port.

The digital part of the IC is fully scan-testable. Two digital inputs, SCANTEST and TEST1, are used for production test: these pins must be left open-circuit in functional mode (correct levels are internally defined by pull-up or pull-down resistors).

8.1 Transmission mode

To provide strict stability with respect to environmental conditions, the carrier frequency is generated by scanning the ROM memory under the control of the microcontroller clock or the reference frequency provided by the on-chip oscillator. High frequency clocking rejects the aliasing components to such an extent that they are filtered by the coupling LC network and do not cause any significant disturbance. The data modulation is applied through pin $\overline{\text{DATA\_IN}}$ and smoothly applied by specific digital circuits to the carrier (shaping). Harmonic components are limited in this process, thus avoiding unacceptable disturbance of the transmission channel (according to CISPR16 and EN50065-1 recommendations). A −55 dB Total Harmonic Distortion (THD) is reached when the typical LC coupling network (or an equivalent filter) is used.

The DAC and the power stage are set in order to provide a maximum signal level of 122 dBμV (RMS) at the output.

The output of the power stage (TX_OUT) must **always** be connected to a decoupling capacitor, because of a DC level of $0.5V_{DD}$ at this pin, which is present even when the device is not transmitting. This pin must also be **protected against overvoltage and negative transient signals**. The DC level of TX_OUT can be used to bias a unipolar transient suppressor, as shown in the application diagram (see Figure 15).

Direct connection to the mains is done through an LC network for low-cost applications. However, an HF signal transformer could be used when power-line insulation has to be performed.

Remark: In transmission mode, the receiving part of the circuit is **not disabled** and the detection of the transmitted signal is normally performed. In this mode, the gain chosen before the beginning of the transmission is stored, and the **AGC is internally set to −6 dB** as long as $\overline{\text{DATA\_IN}}$ is LOW. Then, the old gain setting is **automatically restored**.

8.2 Reception mode

The input signal received by the modem is applied to a wide range input amplifier with AGC (−6 dB to +30 dB). This is basically for noise performance improvement and signal level adjustment, which ensures a maximum sensitivity of the ADC. An 8-bit conversion is then performed, followed by digital band-pass filtering, to meet the CISPR16 normalization and to comply with some additional limitations met in current applications.

After digital demodulation, the baseband data signal is made available after pulse shaping.

The signal pin (RX_IN) is a high-impedance input which has to be protected and DC decoupled for the same reasons as with pin TX_OUT. The high sensitivity (82 dBμV) of this input requires an efficient 50 Hz rejection filter (realized by the LC coupling network), which also acts as an anti-aliasing filter for the internal digital processing; (see Figure 15).

8.3 Data format

8.3.1 Transmission mode

The data input ($\overline{\text{DATA\_IN}}$) is active LOW: this means that a burst is generated on the line (pin TX_OUT) when $\overline{\text{DATA\_IN}}$ pin is LOW.

Pin TX_OUT is in a high-impedance state as long as the device is not transmitting. Successive logic 1s are treated in a Non-Return-to-Zero (NRZ) mode, see pulse shapes in Figure 8 and Figure 9.

8.3.2 Reception mode

The data output (pin $\overline{\text{DATA\_OUT}}$) is active LOW; this means that the data output is LOW when a burst is received. Pin $\overline{\text{DATA\_OUT}}$ remains LOW as long as a burst is received.

8.4 Power-down mode

Power-down input (pin PD) is active HIGH; this means that the power consumption is minimum when pin PD is HIGH. Now, all functions are disabled, except clock generation.

9. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		4.5	5.5	V
f_{osc}	oscillator frequency		-	12	MHz
T_{stg}	storage temperature		–50	+150	°C
T_{amb}	ambient temperature		–50	+100	°C
T_j	junction temperature		-	125	°C

10. Characteristics

Table 5. Characteristics

$V_{DDD} = V_{DDA} = 5\ V \pm 5\ \%$; $T_{amb} = -40\ °C$ to $+85\ °C$; V_{DDD} connected to V_{DDA}; DGND connected to AGND.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{DD}	supply voltage		4.75	5	5.25	V
$I_{DD(tot)}$	total supply current	f_{osc} = 8.48 MHz				
		Reception mode	-	28	38	mA
		Transmission mode; $\overline{DATA\_IN}$ = 0; $Z_L = 30\ \Omega$ [1]	-	47	68	mA
		Power-down mode	-	19	25	mA
$I_{DD(RX/TX)(tot)}$	total analog + digital supply current	$V_{DD} = 5\ V \pm 5\ \%$; Transmission or Reception mode	-	28	38	mA
$I_{DD(PD)(tot)}$	total analog + digital supply current	$V_{DD} = 5\ V \pm 5\ \%$; PD = HIGH; Power-down mode	-	19	25	mA
$I_{DD(PAMP)}$	power amplifier supply current	$V_{DD} = 5\ V \pm 5\ \%$; $Z_L = 30\ \Omega$; $\overline{DATA\_IN}$ = LOW in Transmission mode	-	19	30	mA
$I_{DD(PAMP)(max)}$	maximum power amplifier supply current	$V_{DD} = 5\ V \pm 5\ \%$; $Z_L = 1\ \Omega$; $\overline{DATA\_IN}$ = LOW in Transmission mode	-	76	-	mA
$\overline{DATA\_IN}$ and PD inputs; $\overline{DATA\_OUT}$ and CLK_OUT outputs						
V_{IH}	HIGH-level input voltage		$0.2V_{DD} + 0.9$	-	$V_{DD} + 0.5$	V
V_{IL}	LOW-level input voltage		–0.5	-	$0.2V_{DD} - 0.1$	V
V_{OH}	HIGH-level output voltage	$I_{OH} = -1.6$ mA	2.4	-	-	V
V_{OL}	LOW-level output voltage	$I_{OL} = 1.6$ mA	-	-	0.45	V

Table 5. Characteristics *...continued*

V_{DDD} = V_{DDA} = 5 V ±5 %; T_{amb} = −40 °C to +85 °C; V_{DDD} connected to V_{DDA}; DGND connected to AGND.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OSC1 input and OSC2 output (OSC2 only used for driving external quartz crystal; must be left open-circuit when using an external clock generator)						
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	V_{DD} + 0.5	V
V_{IL}	LOW-level input voltage		−0.5	-	$0.2V_{DD}$ − 0.1	V
V_{OH}	HIGH-level output voltage	I_{OH} = −1.6 mA	2.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 1.6 mA	-	-	0.45	V
Clock						
f_{osc}	oscillator frequency		6.080	-	9.504	MHz
f_{osc}/f_{cr}	ratio between oscillator and carrier frequency		-	64	-	
f_{osc}/f_{CLKOUT}	ratio between oscillator and clock output frequency		-	2	-	
Transmission mode						
f_{cr}	carrier frequency	f_{osc} = 8.48 MHz [2]	-	132.5	-	kHz
t_{su}	set-up time of the shaped burst	f_{osc} = 8.48 MHz; see Figure 8	-	170	-	µs
t_h	hold time of the shaped burst	f_{osc} = 8.48 MHz; see Figure 8	-	170	-	µs
$t_{W(DI)(min)}$	minimum pulse width of $\overline{DATA\_IN}$ signal	f_{osc} = 8.48 MHz; see Figure 8	-	190	-	µs
$V_{o(rms)}$	output carrier signal (RMS value)	$\overline{DATA\_IN}$ = LOW; Z_L = CISPR16	120	-	122	dBµV
$I_{o(max)}$	power amplifier maximum output current (peak value)	$\overline{DATA\_IN}$ = LOW; Z_L = 1 Ω	-	160	-	mA
Z_o	output impedance of the power amplifier		-	5	-	Ω
V_O	output DC level at pin TX_OUT		-	2.5	-	V
THD	total harmonic distortion on CISPR16 load with the coupling network (measured on the first ten harmonics)	$V_{o(rms)}$ = 121 dBµV on CISPR16 load; f_{osc} = 8.48 MHz; $\overline{DATA\_IN}$ = LOW (no modulation); see Figure 3 and Figure 22	-	−55	-	dB
B_{-20dB}	bandwidth of the shaped output signal (at −20 dB) on CISPR16 load with the coupling network	$V_{o(rms)}$ = 121 dBµV on CISPR16 load; f_{osc} = 8.48 MHz; $\overline{DATA\_IN}$ = 300 Hz; duty factor = 50 %; see Figure 4	-	3000	-	Hz

Table 5. Characteristics *…continued*

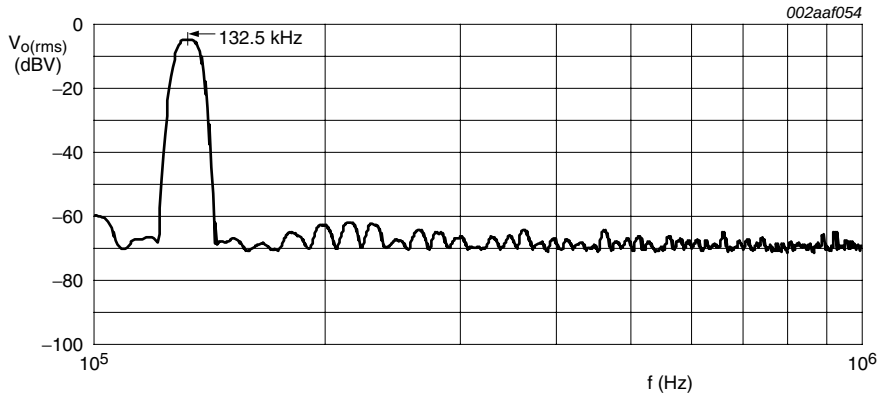
V_{DDD} = V_{DDA} = 5 V ± 5 %; T_{amb} = −40 °C to +85 °C; V_{DDD} connected to V_{DDA}; DGND connected to AGND.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Reception mode						
$V_{i(rms)}$	analog input signal (RMS value)	[3]	82	-	122	dBμV
V_I	DC level at pin RX_IN		-	2.5	-	V
Z_i	RX_IN input impedance		-	50	-	kΩ
R_{AGC}	AGC range		-	36	-	dB
$t_{c(AGC)}$	AGC time constant	f_{osc} = 8.48 MHz; see Figure 5	-	296	-	μs
$t_{d(dem)(su)}$	demodulation delay set-up time	f_{osc} = 8.48 MHz; see Figure 21	-	350	400	μs
$t_{d(dem)(h)}$	demodulation delay hold time	f_{osc} = 8.48 MHz; see Figure 21	-	420	470	μs
B_{det}	detection bandwidth	f_{osc} = 8.48 MHz	-	3	-	kHz
BER	bit error rate	f_{osc} = 8.48 MHz; 600 baud; S/N = 35 dB; signal 76 dBμV; see Figure 23	-	1	-	1×10^{-4}
Power-up timing						
$t_{d(pu)(TX)}$	delay between power-up and DATA_IN in transmission mode	XTAL = 8.48 MHz; C1 = C2 = 27 pF; R_p = 2.2 MΩ; see Figure 10	-	1	-	μs
$t_{d(pu)(RX)}$	delay between power-up and DATA_OUT in reception mode	XTAL = 8.48 MHz; C1 = C2 = 27 pF; R_p = 2.2 MΩ; f_{RXIN} = 132.5 kHz; 120 dBμV sine wave; see Figure 11	-	1	-	μs
Power-down timing						
$t_{d(pd)(TX)}$	delay between PD = 0 and DATA_IN in transmission mode	f_{osc} = 8.48 MHz; see Figure 12	-	10	-	μs
$t_{d(pd)(RX)}$	delay between PD = 0 and DATA_OUT in reception mode	f_{osc} = 8.48 MHz; f_{RXIN} = 132.5 kHz; 120 dBμV sine wave; see Figure 13	-	500	-	μs
$t_{active(min)}$	minimum active time with T = 10 ms power-down period in reception mode	f_{osc} = 8.48 MHz; f_{RXIN} = 132.5 kHz; 120 dBμV sine wave; see Figure 14	-	1	-	μs

[1] The value of the total transmission mode current is the sum of $I_{DD(RX/TX)(tot)}$ + $I_{DD(PAMP)}$.

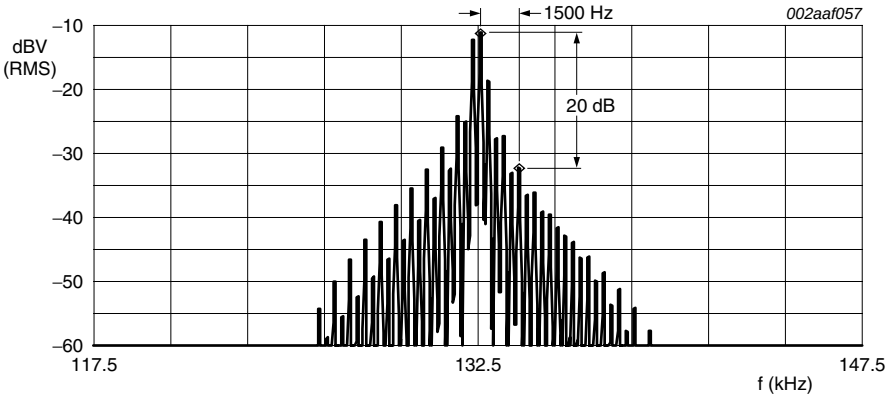
[2] Frequency range corresponding to the EN50065-1 band. However, the modem can operate at any lower oscillator frequency.

[3] The minimum value can be improved by using an external amplifier; see application diagrams Figure 19 and Figure 20.



Resolution bandwidth = 9 kHz; top: 0 dBV (RMS) = 120 dBμV (RMS); marker at −5 dBV (RMS) = 115 dBμV (RMS); the CISPR16 network provides an attenuation of 6 dB, so the signal amplitude is 121 dBμV (RMS).

Fig 3. Carrier spectrum



Resolution bandwidth = 100 Hz; B_{-20dB} = 3000 Hz (2 × 1500 Hz).

Fig 4. Shaped signal spectrum

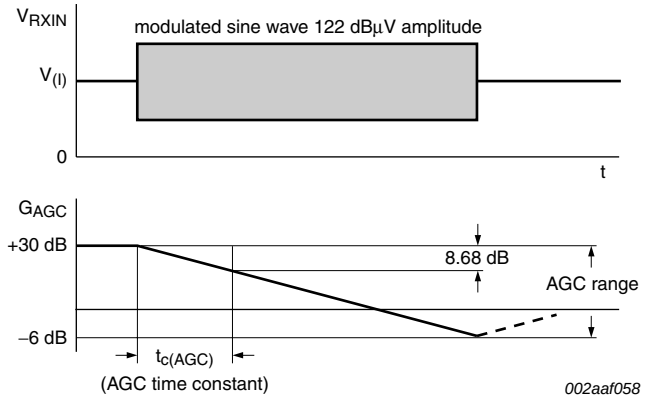
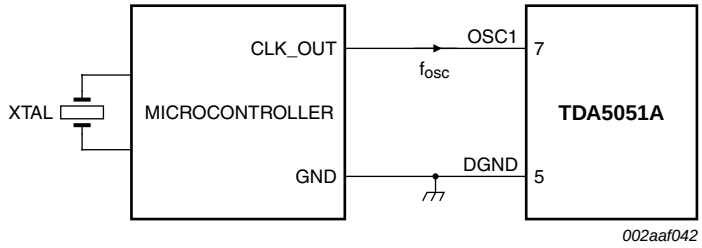


Fig 5. AGC time constant definition (not to scale)

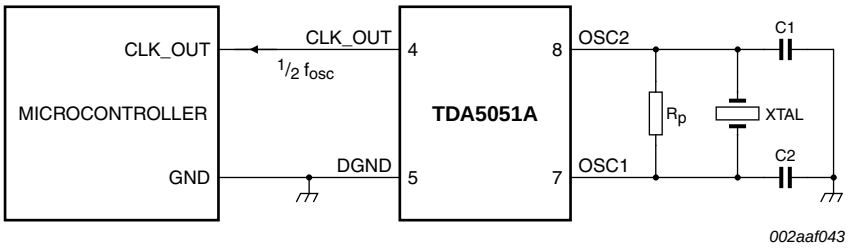
11. Timing

11.1 Configuration for clock



For parameter description, see Table 6.

Fig 6. External clock



For parameter description, see Table 6.

Fig 7. Typical configuration for on-chip clock circuit

Table 6. Clock oscillator parameters

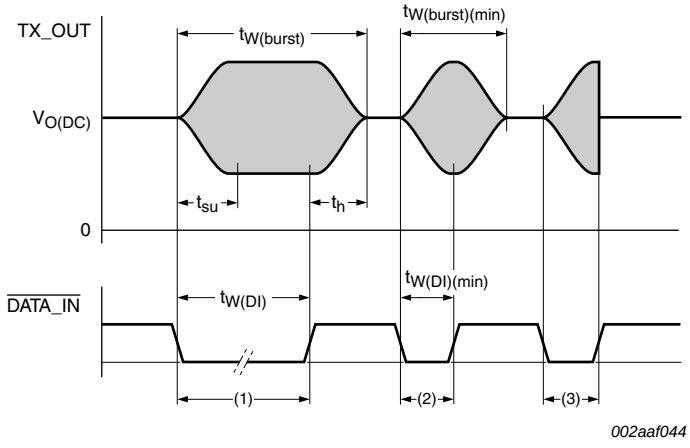
Oscillator frequency f_{osc}	Carrier frequency f_{cr}	Clock output frequency $\frac{1}{2}f_{osc}$	External components
6.080 MHz to 9.504 MHz	95 kHz to 148.5 kHz	3.040 MHz to 4.752 MHz	C1 = C2 = 27 pF to 47 pF; R_p = 2.2 MΩ to 4.7 MΩ; XTAL = standard quartz crystal

Table 7. Calculation of parameters depending on the clock frequency

Symbol	Parameter	Conditions	Unit
f_{osc}	oscillator frequency	with on-chip oscillator: frequency of the crystal quartz	Hz
		with external clock: frequency of the signal applied at OSC1	Hz
f_{CLKOUT}	clock output frequency	$\frac{1}{2}f_{osc}$	Hz
f_{cr}	carrier frequency/digital filter tuning frequency	$\frac{1}{64}f_{osc}$	Hz
t_{su}	set-up time of the shaped burst	$23/f_{cr}$ or $1472/f_{osc}$	s
t_h	hold time of the shaped burst	$23/f_{cr}$ or $1472/f_{osc}$	s
$t_{W(DI)(min)}$	minimum pulse width of $\overline{DATA\_IN}$ signal	$t_{su} + 1/f_{cr}$	s

Table 7. Calculation of parameters depending on the clock frequency *…continued*

Symbol	Parameter	Conditions	Unit
$t_{W(burst)(min)}$	minimum burst time of $V_{O(DC)}$ signal	$t_{W(DI)(min)} + t_h$	s
$t_{c(AGC)}$	AGC time constant	$2514/f_{osc}$	s
$t_{su(demod)}$	demodulation set-up time	$3200/f_{osc}$ (max.)	s
$t_{h(demod)}$	demodulation hold time	$3800/f_{osc}$ (≈max.)	s



(1) $t_{W(DI)} > t_{W(DI)(min)}$

(2) $t_{W(DI)(min)} = t_{su} + 1/f_{cr}$

(3) $t_{W(DI)(min)} < t_{su}$; wrong operation

Fig 8. Relationship between $\overline{\text{DATA\_IN}}$ and TX_OUT (see Table 8)

Table 8. Relationship between $\overline{\text{DATA\_IN}}$ and TX_OUT

X = don't care.

PD	$\overline{\text{DATA\_IN}}$	TX_OUT
1	X	high-impedance
0	1	high-impedance (after t_h)
0	0	active with DC offset

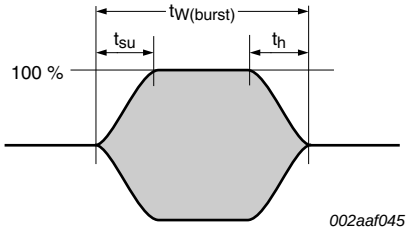
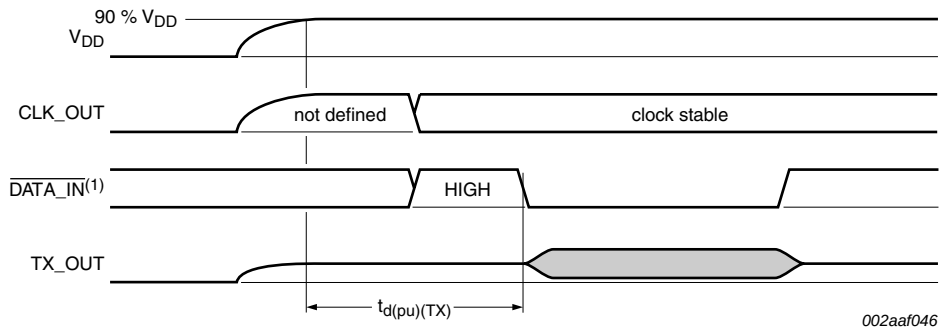


Fig 9. Pulse shape characteristics

11.2 Timing diagrams



(1) $\overline{\text{DATA\_IN}}$ is an edge-sensitive input and must be HIGH before starting a transmission.

Fig 10. Timing diagram during power-up in Transmission mode

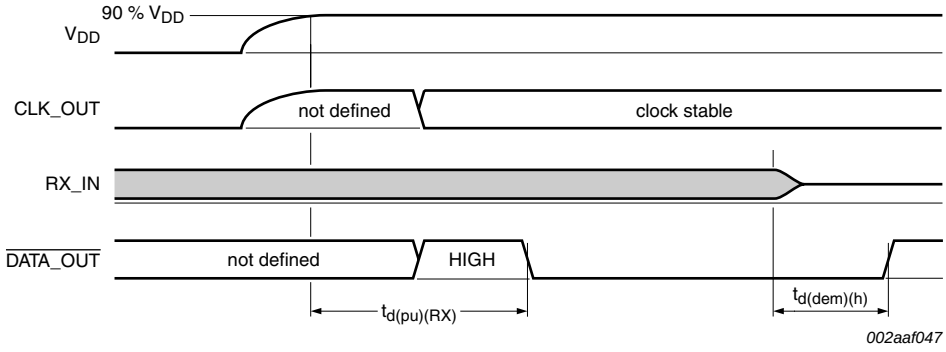


Fig 11. Timing diagram during power-up in Reception mode

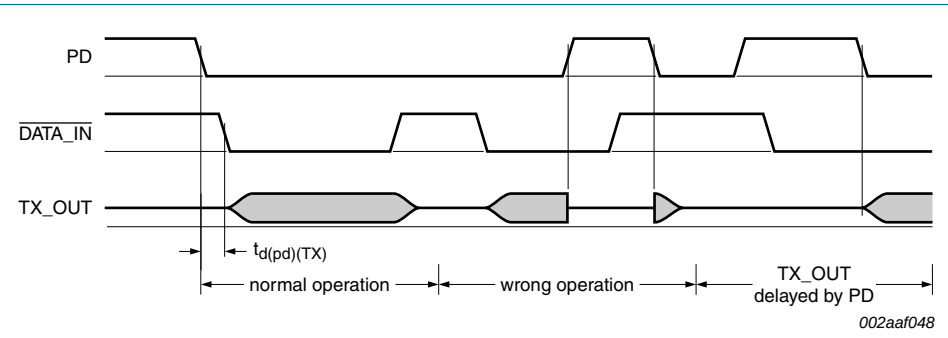


Fig 12. Power-down sequence in Transmission mode

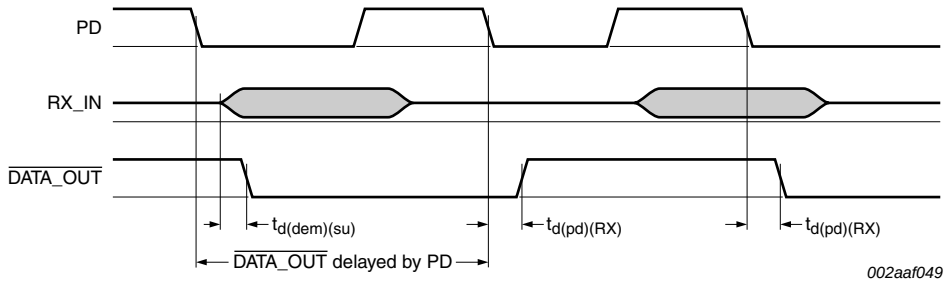


Fig 13. Power-down sequence in Reception mode

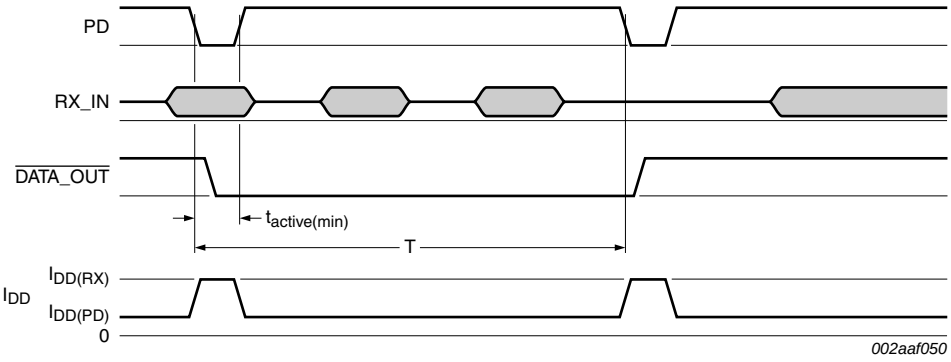
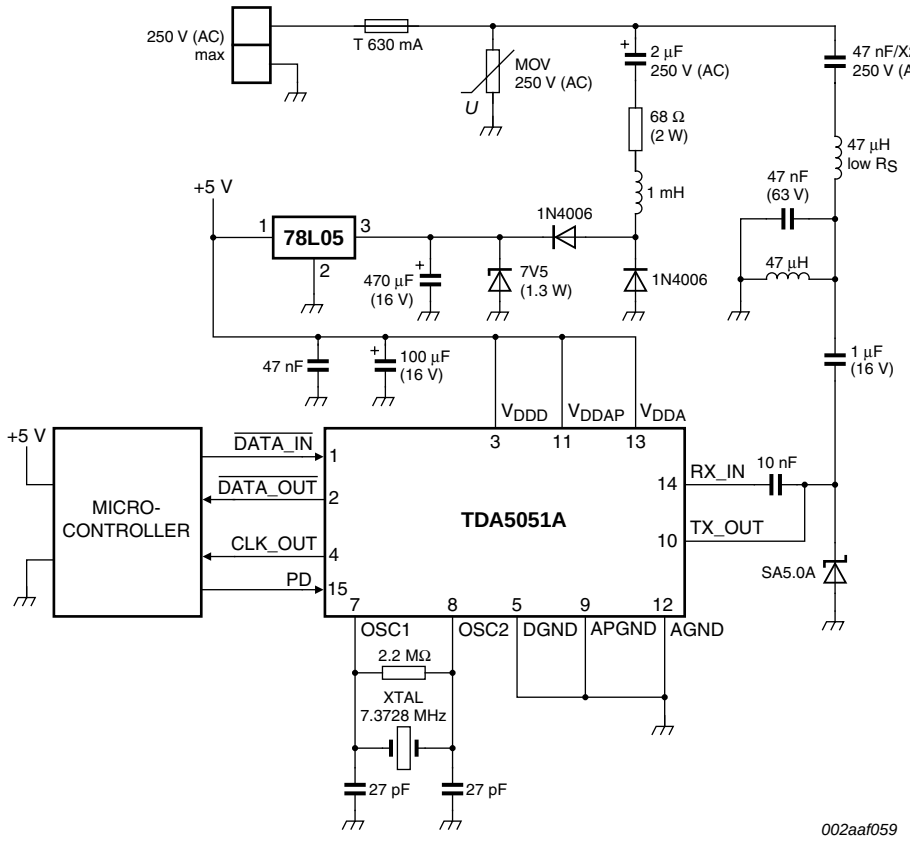


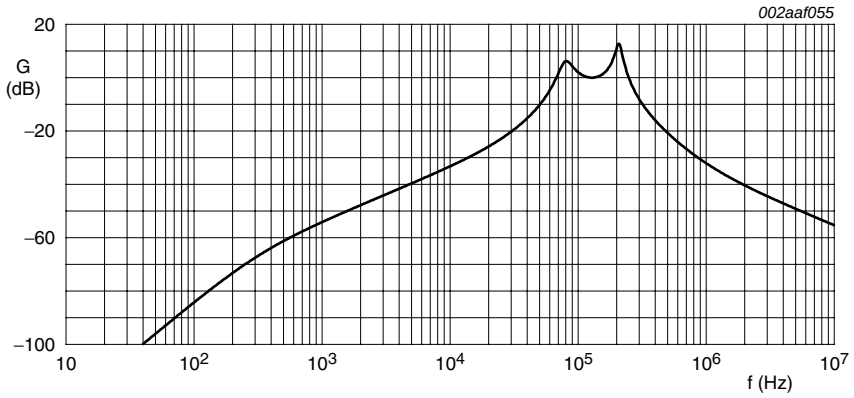
Fig 14. Power saving by dynamic control of power-down

12. Application information

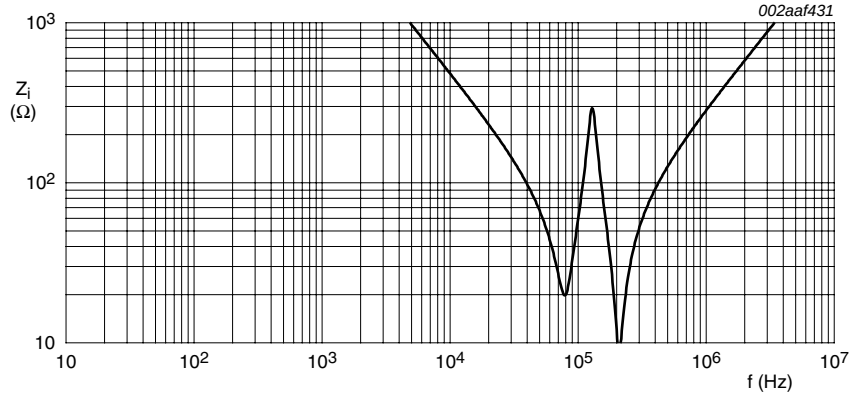


f_{cr} = 115.2 kHz for XTAL = 7.3728 MHz standard crystal.

Fig 15. Application diagram without power line insulation



a. Gain

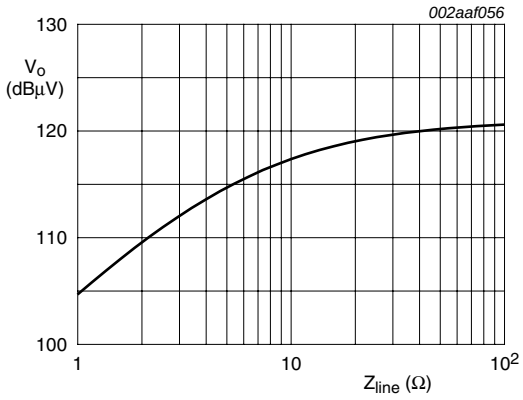


b. Input impedance

f_{cr} = 115.2 kHz; L = 47 μH; C = 47 nF.

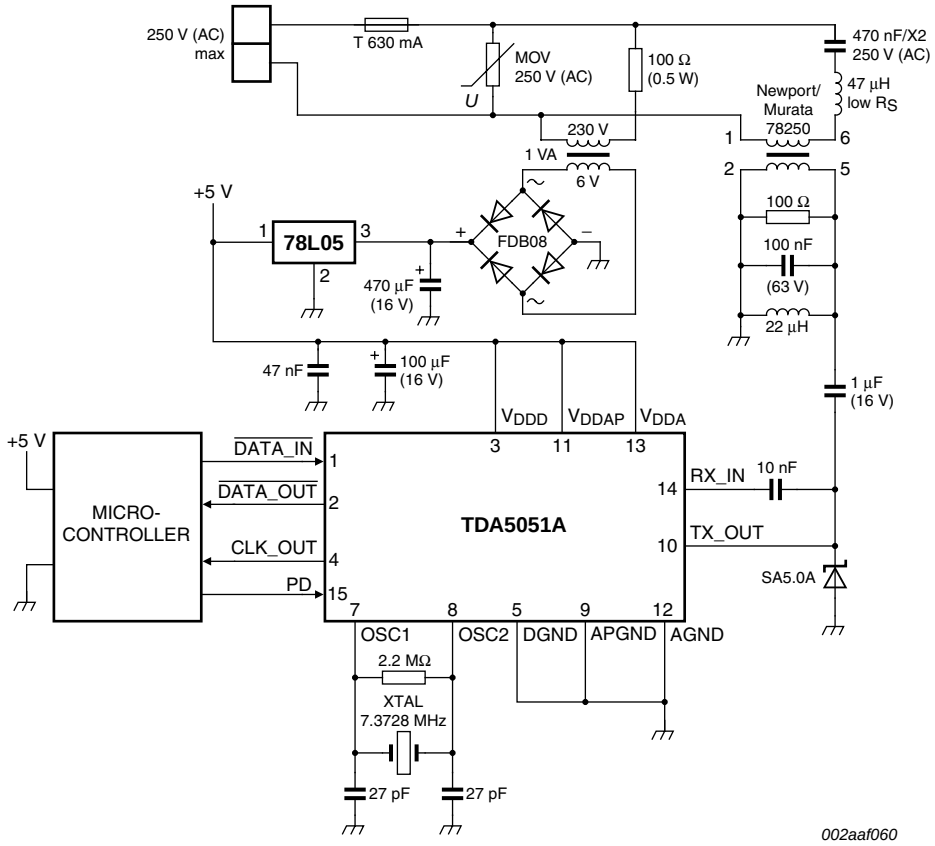
Main features of the coupling network: 50 Hz rejection > 80 dB; anti-aliasing for the digital filter > 50 dB at the sampling frequency ($\frac{1}{2}f_{osc}$). Input impedance always higher than 10 Ω within the 95 kHz to 148.5 kHz band.

Fig 16. Gain (a) and input impedance (b) of the coupling network



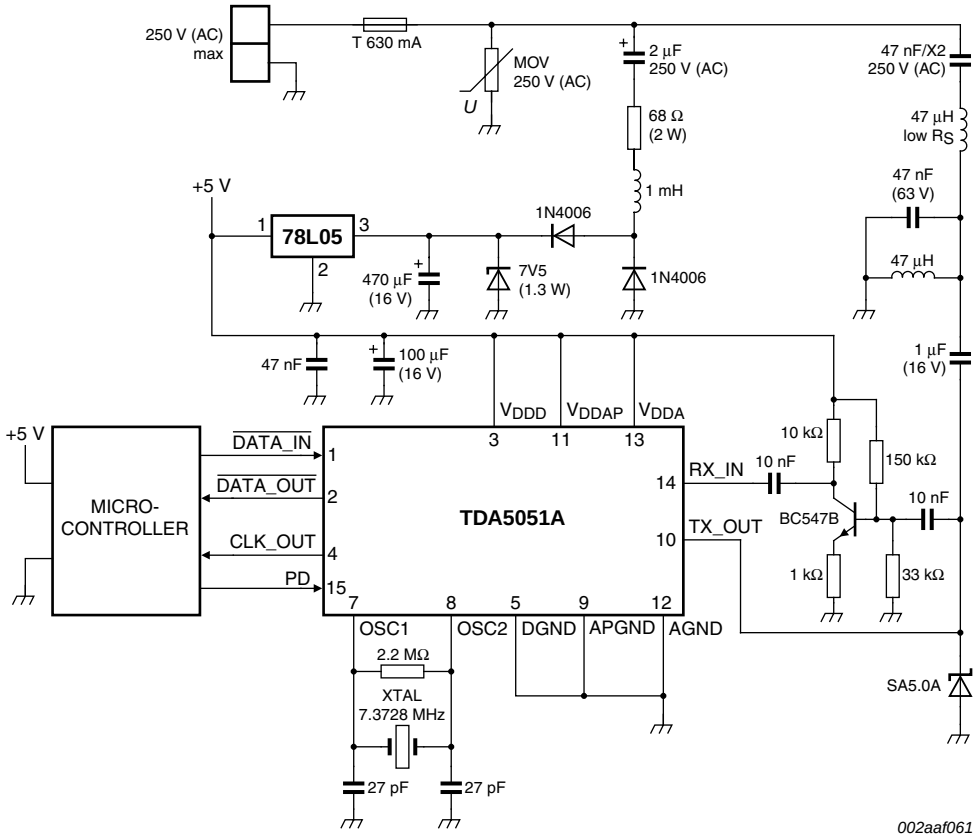
with coupling network; L = 47 μH; C = 47 nF.

Fig 17. Output voltage as a function of line impedance



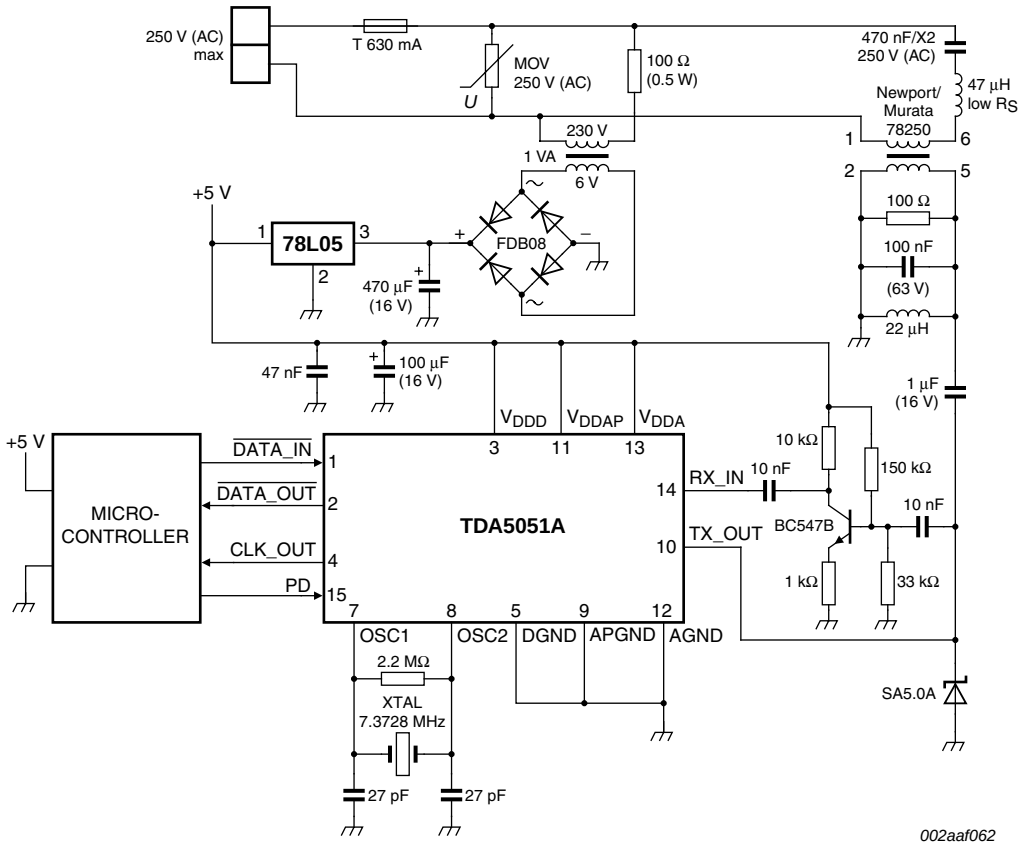
f_{cr} = 115.2 kHz for XTAL = 7.3728 MHz standard crystal.

Fig 18. Application diagram with power line insulation



f_{cr} = 115.2 kHz for XTAL = 7.3728 MHz standard crystal.

Fig 19. Application diagram without power line insulation, with improved sensitivity (68 dBµV typ.)



f_{cr} = 115.2 kHz for XTAL = 7.3728 MHz standard crystal.

Fig 20. Application diagram with power line insulation, with improved sensitivity (68 dBµV typ.)

13. Test information

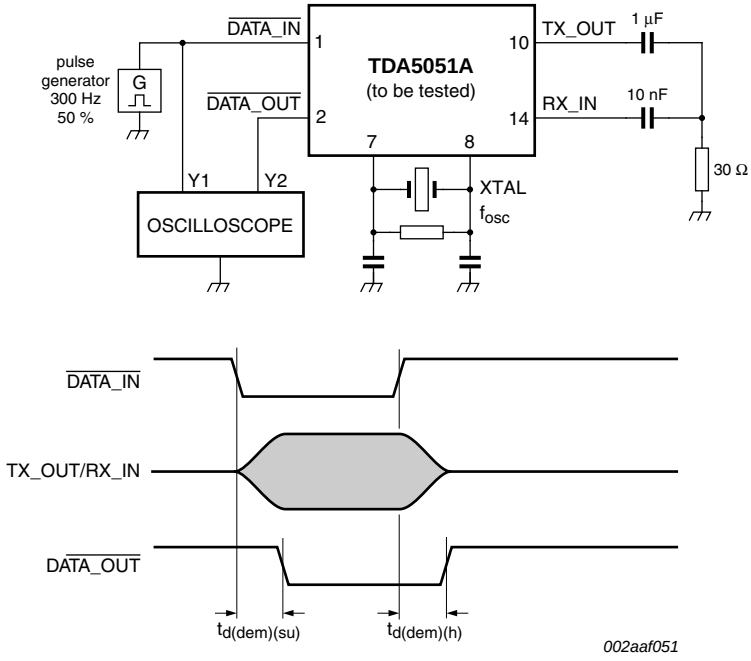
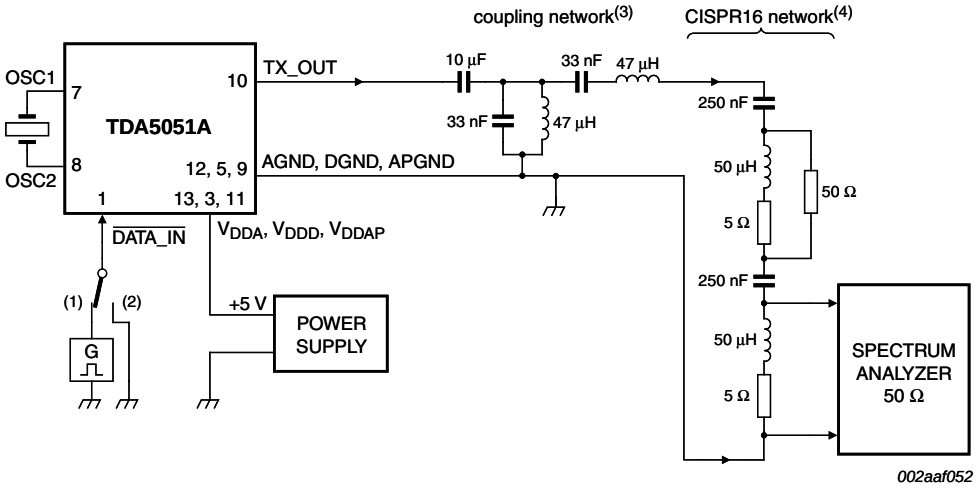


Fig 21. Test set-up for measuring demodulation delay



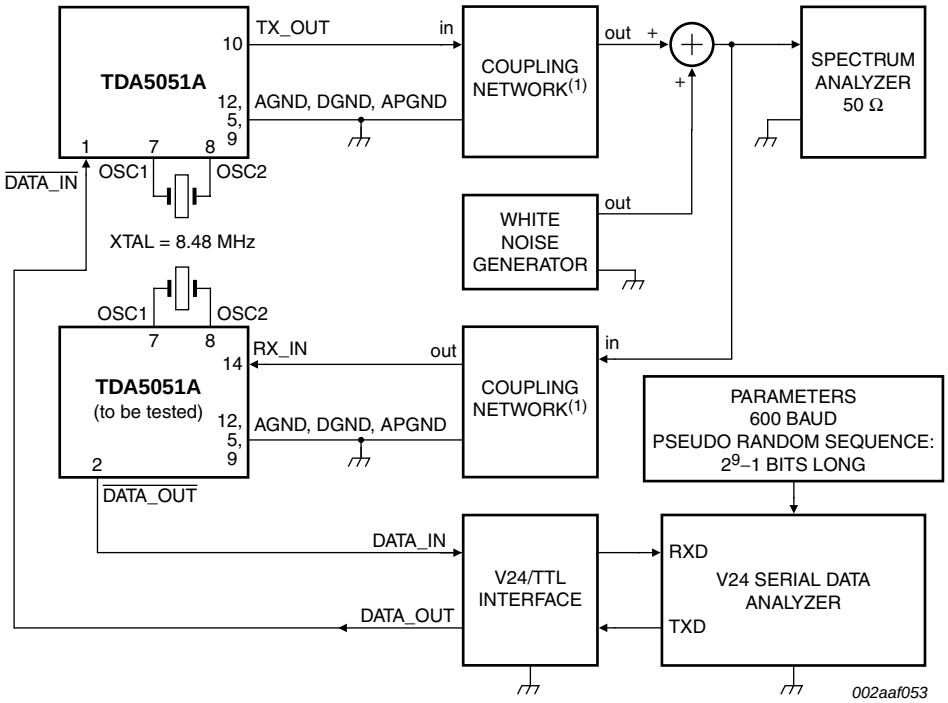
(1) Square wave TTL signal 300 Hz, duty factor = 50 % for measuring signal bandwidth (see Figure 3).

(2) $\overline{\text{DATA\_IN}}$ + LOW for measuring total harmonic distortion (see Figure 3).

(3) Tuned for f_{cr} = 132.5 kHz.

(4) The CISPR16 network provides a −6 dB attenuation.

Fig 22. Test set-up for measuring THD and bandwidth of the TX_OUT signal

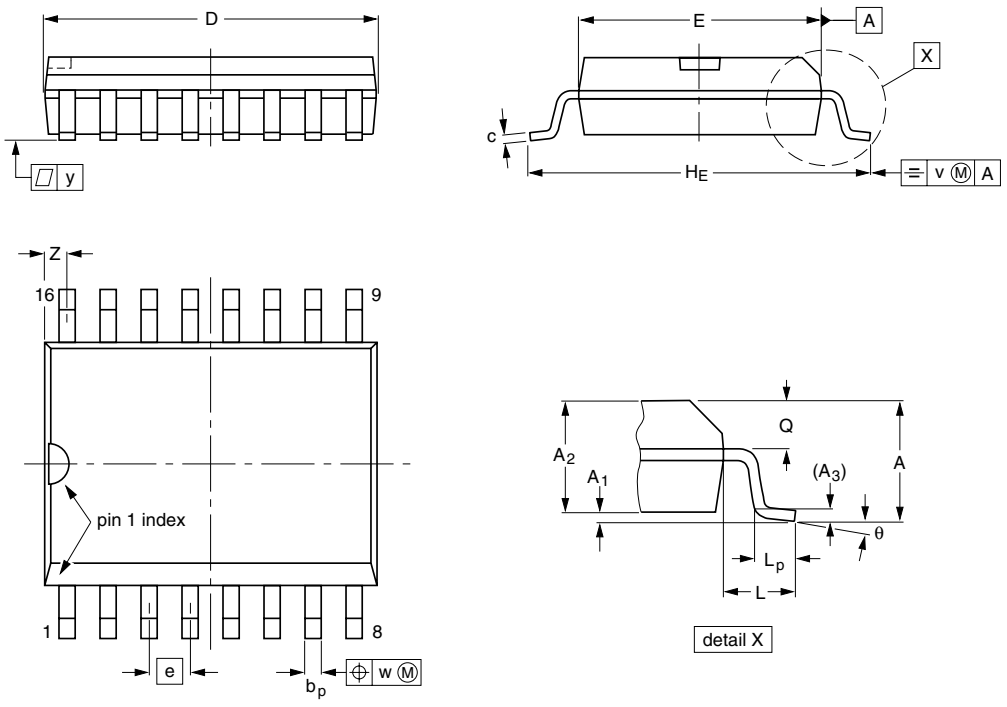


(1) See Figure 22.

Fig 23. Test set-up for measuring Bit Error Rate (BER)

14. Package outline

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT162-1	075E03	MS-013				~~99-12-27~~ 03-02-19

Fig 24. Package outline SOT162-1 (SO16)

15. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 25) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 9 and 10

Table 9. SnPb eutectic process (from J-STD-020C)

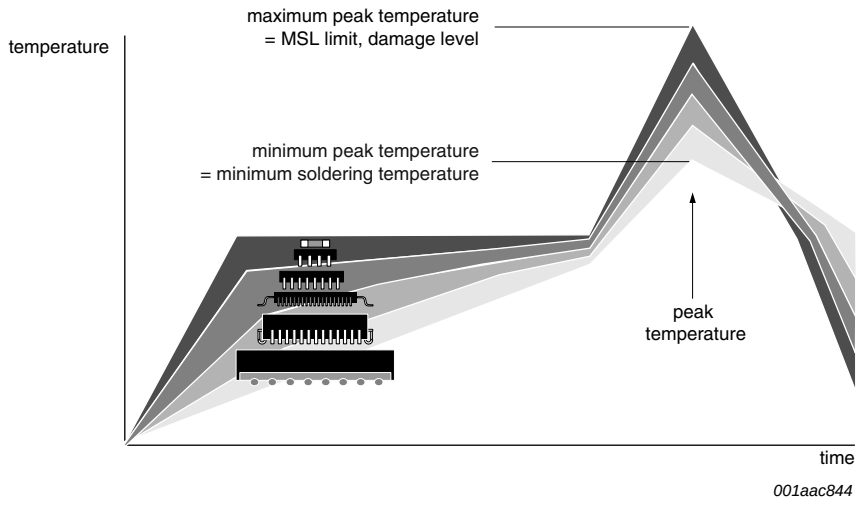
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 10. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 25.



MSL: Moisture Sensitivity Level

Fig 25. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. Abbreviations

Table 11. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
ASK	Amplitude Shift Keying
CMOS	Complementary Metal-Oxide Semiconductor
DAC	Digital-to-Analog Converter
HF	High-Frequency
I/O	Input/Output
IC	Integrated Circuit
LC	inductor-capacitor filter
NRZ	Non-Return-to-Zero
RMS	Root Mean Squared
ROM	Read-Only Memory
THD	Total Harmonic Distortion
TTL	Transistor-Transistor Logic

18. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA5051A v.5	20110113	Product data sheet	-	TDA5051A v.4
Modifications:	• Table 1 “Quick reference data”, T_{amb}, ambient temperature: – Min value changed from −10 °C to −50 °C – Max value changed from +80 °C to +100 °C • Table 4 “Limiting values”, T_{amb}, ambient temperature: – Min value changed from −10 °C to −50 °C – Max value changed from +80 °C to +100 °C • Table 5 “Characteristics”, descriptive line below title is changed from “T_{amb} = 0 °C to 70 °C” to “T_{amb} = −40 °C to +85 °C”			
TDA5051A v.4	20100701	Product data sheet	-	TDA5051A v.3
TDA5051A v.3	20100422	Preliminary data sheet	-	TDA5051A v.2
TDA5051A v.2 (9397 750 05035)	19990531	Product specification	-	TDA5051A v.1
TDA5051A v.1 (9397 750 02571)	19970919	Product specification	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

19.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

19.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

19.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

20. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

21. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 13 January 2011
Document identifier: TDA5051A

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

NXP:

TDA5051AT/C1,512 TDA5051AT/C1,518