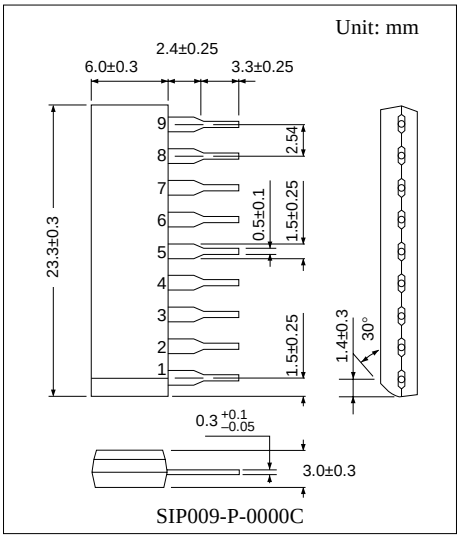
AN8027, AN8037

AC-DC switching power supply control IC with standby mode

■ Overview

The AN8027 and AN8037 are ICs developed for self-excited switching regulator of RCC local resonance control type.

These ICs are designed to achieve stability and high efficiency over a wide input voltage range and loads range (light loads to heavy loads), for supporting input levels used worldwide and improved conformance with energy conservation laws.



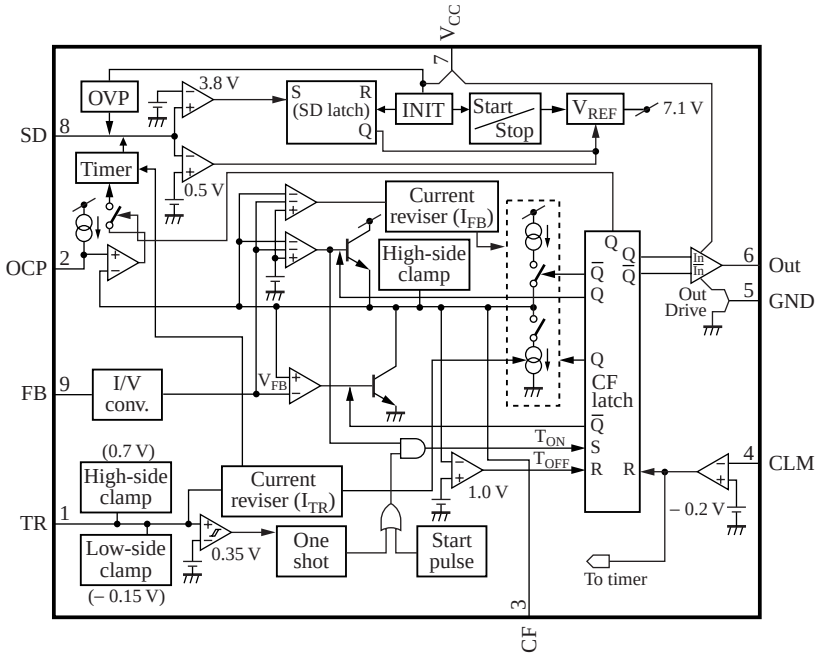
■ Features

- Support improved conformance with energy conservation laws by providing two operating modes.
  - Standby mode (light loads):
    Achieves better efficiency due to reduced frequency .
  - Normal mode:
    Achieves high efficiency in RCC local resonance operation with zero-cross detection.
- Incorporating an input voltage compensation function available to a wide input range for worldwide use.
  - This function compensates the maximum on-period in inverse proportion to the input voltage.
- Incorporating a timer latch function.
  - The time period can be adjusted according to the overload in normal mode or standby mode.
  - This function makes it possible to protect the IC from damage that may be caused by the short-circuiting of the IC's external capacitor for the timer.
- Incorporating an overvoltage protection function. (detects at V_{CC} pin)
- Incorporating a pulse-by-pulse overcurrent protection function, which makes latch protection possible at the time of the short-circuiting of the transformer's primary winding.
- Adopting a 9-pin single inline package (E-9S: available to manufacturing in overseas).
- AN8027: Transformer resetting is detected from the high- or low-level signal on the TR pin.
- AN8037: Transformer resetting is detected from the falling edge of the high-level signal on the TR pin.
  Refer to the "[1] operation descriptions 7. local resonance operation" section in the application notes.

■ Applications

- Televisions, VCRs, facsimiles, and printers

■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	24	V
Constant output current	I_{OUT}	±150	mA
Peak output current	I_{OP}	±1 000	mA
TR pin allowable application current	I_{TR}	±5	mA
OCP pin allowable application voltage	V_{OCP}	– 0.3 to +7.0	V
CLM pin allowable application voltage	V_{CLM}	– 0.3 to +7.0	V
SD pin allowable application voltage	V_{SD}	– 0.3 to +7.0	V
FB pin allowable application current	I_{FB}	0 to –2.0	mA
Power dissipation ($T_a \leq 25°C$)	P_D	874	mW
Power dissipation ($T_a = 85°C$)		454	mW
Operating ambient temperature *	T_{opr}	–30 to +85	°C
Storage temperature *	T_{stg}	–55 to +150	°C

Note) 1. *: Except for the operating ambient temperature and storage temperature, all ratings are for $T_a = 25°C$.

2. Do not apply external currents or voltages to any pins not specifically mentioned.
For circuit current, '+' denotes current flowing into the IC, and '–' denotes current flowing out of the IC.

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC}	From the stop voltage to the OVP supply voltage	V

■ Electrical Characteristics at V_{CC} = 18 V, T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Low voltage protection (U.V.L.O.) initial startup supply voltage	$V_{CC-START}$		13.4	14.9	16.4	V
Low voltage protection (U.V.L.O.) operation stop supply voltage	$V_{CC-STOP}$		7.7	8.6	9.5	V
Overvoltage protection (OVP) operating supply voltage	V_{CC-OVP}		19.4	20.5	21.6	V
Overvoltage protection (SD) operating threshold voltage	V_{TH1-SD}		3.5	3.9	4.3	V
Overvoltage protection (SD) reset threshold voltage	V_{TH2-SD}		0.4	0.8	1.2	V
Remote (RM) operating threshold voltage	V_{TH1-RM}		0.05	0.15	0.3	V
Shutdown (SD) standby voltage	V_{STB-SD}	SD pin = Open	1.0	1.5	2.0	V
Overvoltage protection (OVP) reset supply voltage	$V_{CC-OVPC}$		7.3	8.1	8.9	V
Remote (RM) operating time circuit current	I_{CC-RM}	V_{CC} = 18 V, V_{SD} = 0 V	3.0	4.0	5.0	mA
Overvoltage protection (SD) operating time circuit current 1	I_{CC1-SD}	V_{CC} = 10 V, V_{SD} = 4.3 V → Open	1.2	1.5	1.8	mA
Overvoltage protection (SD) operating time circuit current 2	I_{CC2-SD}	V_{CC} = 18 V, V_{SD} = 4.3 V → Open	3.6	4.5	5.4	mA
Timer latch (SD) charge current 1	$I_{SD1-TIM}$	FB pin = Open, I_{TR} = –270 µA	68	102	136	µA
Timer latch (SD) charge current 2	$I_{SD2-TIM}$	FB pin = Open, I_{TR} = –1.64 mA	179	267	355	µA
Timer latch (SD) start feedback current	I_{FB-TIM}	I_{TR} = –1 mA, R_{OCP} = 30 kΩ	– 0.95	– 0.75	– 0.55	mA
Transformer reset detection (TR) threshold voltage	V_{TH-TR}		0.15	0.25	0.35	V
Transformer reset detection (TR) upper limit clamp voltage	V_{CLH-TR}	I_{TR} = 3 mA	0.55	0.7	0.85	V
Transformer reset detection (TR) lower limit clamp voltage	V_{CLL-TR}	I_{TR} = –3 mA	– 0.3	– 0.15	0	V
Overcurrent protection (CLM) threshold voltage	V_{TH-CLM}		–220	–200	–180	mV
Oscillator (CF) upper limit voltage	V_{H-CF}	FB pin = Open, C_F = 2 200 pF	3.8	4.2	4.6	V
Oscillator (CF) lower limit voltage 1	V_{L1-CF}	FB pin = Open, C_F = 2 200 pF	0.8	1.0	1.2	V
Oscillator (CF) lower limit voltage 2	V_{L2-CF}	I_{FB} = – 0.5 mA, C_F = 2 200 pF	0	0.1	0.3	V
Oscillator (CF) maximum on-period current gain	G_{ION-CF}	FB pin = Open, I_{TR} = –750 µA	0.8	1.0	1.2	—
Oscillator (CF) maximum on-period current	I_{ON-CF}	I_{TR} = 0 mA	200	250	300	µA
Oscillator (CF) minmum off-period current 1	$I_{OFF1-CF}$	I_{FB} = – 0.4 mA	–880	–660	–440	µA

■ Electrical Characteristics at V_{CC} = 18 V, T_a = 25°C (continued)

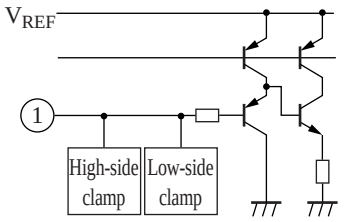
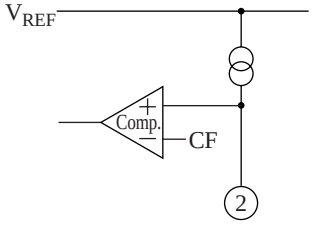
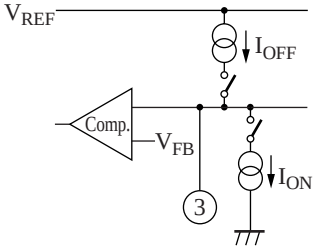
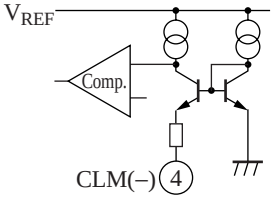
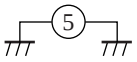
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Oscillator (CF) minmum off-period current 2	$I_{OFF2-CF}$	I_{FB} = – 0.8 mA	–210	–160	–110	µA
Minimun off-period threshold feedback current	$I_{FB-TOFF}$		– 0.78	– 0.6	– 0.42	mA
Overcurrent protection (OCP) pin source current	$I_{OCP-OCP}$		–130	–100	–70	µA
Output oscillator frequency	F_{OSC}	C_F = 2 200 pF, I_{TR} = 475 µA, I_{FB} = – 0.5 mA	50	65	80	kHz
Pre-startup low-level output voltage	V_{OL-STB}	V_{CC} = 13.5 V, I_{OUT} = 1 mA	—	1.0	1.25	V
Low-level output voltage	V_{OL}	I_{OUT} = 0.1 A	—	0.9	2.0	V
High-lebel output voltage	V_{OH}	I_{OUT} = – 0.1 A	15.5	16.3	—	V
Pre-startup circuit current 1	$I_{CC-STB1}$	V_{CC} = 13.5 V	75	100	125	µA
Circuit current 1	$I_{CC1-OPR1}$	V_{CC} = 10 V	8.5	11.5	14.5	mA
Circuit current 2	$I_{CC2-OPR2}$	V_{CC} = 18 V	9.0	12.0	15.0	mA
Circuit current durring startup 1	I_{START1}		—	200	380	µA

• Design reference data

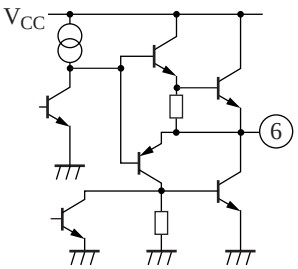
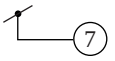
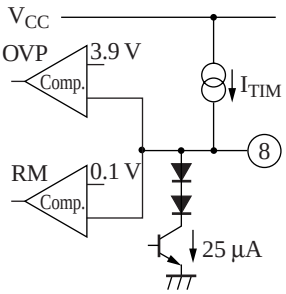
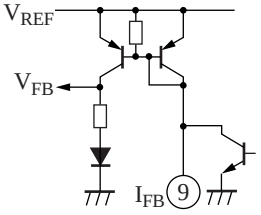
Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Low voltage protection (U.V.L.O.) start/stop supply voltage difference	ΔV_{CC}		—	6.3	—	V
Remote (RM) reset threshold voltage	V_{TH2-RM}		—	0.1	—	V
Timer latch (SD) overcurrent protection time	T_{CLM-SD}		—	0.1	—	s
Transformer reset detection (TR) threshold hysteresis width	ΔV_{TH-TR}		—	0.05	—	V
Maximum on-period	$T_{ON(max)}$	I_{TR} = 0 mA, I_{FB} = – 0.2 mA	—	26.5	—	µs
Minimum off-period	$T_{OFF(min)}$	I_{TR} = 0 mA, I_{FB} = – 0.2 mA	—	5	—	µs
Overcurrent protection (OCP) power-on charge period	$T_{SD(ON)-OCP}$	I_{FB} = – 0.5 mA, R_{OCP} = 22 kΩ	—	1.8	—	µs
Overcurrent protection (OCP) power-off charge period	$T_{SD(OFF)-OCP}$	I_{FB} = – 0.5 mA, R_{OCP} = 30 kΩ	—	8.8	—	µs
Output rise time	t_r	10% to 90%, I_{OUT} = 0 mA	—	60	—	ns
Output fall time	t_f	10% to 90%, I_{OUT} = 0 mA	—	20	—	ns
TR output response time	T_{TR}		—	800	—	ns
CLM output response time	T_{CLM}		—	100	—	ns
Pre-startup circuit current 2	$I_{CC-STB2}$	V_{CC} = 13.5 V, T_a = –30°C to +85°C	50	100	150	µA
Only for AN8037						
Timer period during startup	T_{START}		—	100	—	µs

■ Pin Descriptions

Pin No.	Pin name	I/O	Explanation	Equivalent Circuit
1	TR	I	Transformer reset detection input. When the IC detects transformer resetting and the falling edge of a high-level signal is input to this pin of the AN8037 or a low-level signal is input to the same pin of the AN8027, the level of the Out pin becomes high. However, the transformer reset signal is ignored if the signal is shorter than the minimum off-period determined by the CF pin. Also note that the maximum on-period is corrected according to the source currents.	
2	OCP	—	Connection for the resistor that determines the overload level of the IC to activate the timer latch protection circuit. By judging the operating mode (i.e., the normal or standby mode) of the IC from the secondary side, the timer period is adjusted with the selection of external resistance according to the operating mode.	
3	CF	—	Connection for the capacitor that determines the on- and off-periods of the IC output (Out). The on- and off-periods are corrected by I_{ON} which is proportional to the flowing out current at the TR pin, and I_{OFF} which corresponds to the current at FB pin.	
4	CLM	I	Input to the pulse-by-pulse overcurrent protection circuit. Normally, we recommend adding an external filter for this input. If overcurrent continues for several cycles, the IC determines that the operation is erroneous, thus triggering the latch protection function.	
5	GND	—	IC ground.	

■ Pin Descriptions (continued)

Pin No.	Pin name	I/O	Explanation	Equivalent Circuit
6	Out	O	Output used to directly drive a power MOSFET. A totem pole structure is adopted in this output circuit. The absolute maximum ratings for the output current are: Peak: ±1 A DC: ±150 mA	
7	V_{CC}	—	Power supply. This pin monitors supply voltage and has the threshold for the start, stop, OVP, and OVP reset levels.	
8	SD	I	This pin is used in RM (remote), OVP (overvoltage protection), and timer latch. RM: The IC is in remote operation if this pin is short-circuited to the ground and the output of the IC is turned off. OVP: When overvoltage signal of the power supply is detected and high is inputted to the terminal, it turns off the internal circuit. At the same time, it holds that condition (latch). Timer latch: It detects the output voltage fall due to the overcurrent condition of the power supply output through the current level inputted to FB. When the I_{FB} decreases under the current of certain value, the charge current flows in the capacitor which is connected to this terminal. Then, when the capacitor is charged up to the threshold voltage of the OVP, the OVP works so that the IC could keep the operation stop condition.	
9	FB	I	Connection for the photocoupler used for the power supply output error-voltage feedback. This input can decrease the photocoupler dark current by about 200 µA.	

■ Application Notes

[1] Operation descriptions

1. Start/stop circuit block

- Startup mechanism

After the AC voltage is applied and the supply voltage due to the current in the startup resistor reaches the startup voltage and the IC begins to operate, drive of the power MOSFET begins. This causes a bias in the transformer, and the supply voltage is provided to the IC from the bias winding. (This is point a in figure 1.) During the period between the point when the startup voltage is reached, and the point when the bias winding can generate a voltage enough to supply the IC, the IC supply voltage is provided by the capacitor (C8) connected to V_{CC}. Since the supply voltage falls during this period (area b in figure 1), if the supply voltage falls below the IC stop-voltage before an adequate supply voltage can be provided by the bias winding, it will not be possible to start the power supply. (This is the state at point c in figure 1.)

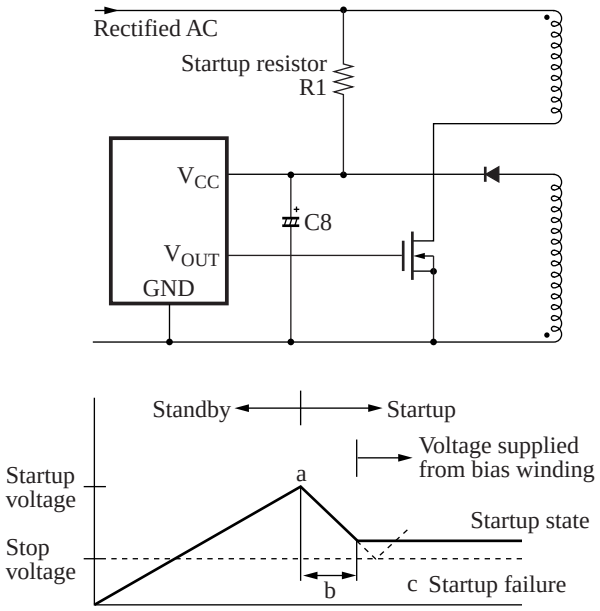


Figure 1

- Functions

This IC includes a function that monitors the V_{CC} voltage. It starts IC operation when V_{CC} reaches the startup voltage (14.9 V typical), and stops operation when the voltage falls below the stop voltage (8.6 V typical). Since a large voltage difference (6.3 V typical) is taken between the start and stop voltages, it is easy to select values for the start resistor and the capacitor connected to V_{CC} .

Note) To start up the IC operation, the startup current which is a pre-start current plus a circuit drive current is necessary. Set the resistance value so as to supply a startup current of 400 µA.

2. Oscillation circuit

The oscillation circuit makes use of the charge and discharge of current to and from the capacitor C_{CF} connected to the CF pin (pin 3) to determine the switching timing of the power MOSFET.

The IC is in constant voltage control by changing the on-period of the power MOSFET without making off-period change while the IC is in normal (RCC continuous) operation mode. At that time, the on-period is controlled by directly changing the output pulse width of the oscillation circuit, and the maximum on-period can be adjusted with input voltage compensation by detecting the input voltage with the flow of current from the TR pin (TR source current). Refer to figure 2. When the IC is in standby mode (for light loads), the stable, efficient control of the IC is ensured by detecting the flow of current from the FB pin (I_{FB}) and changing the off-period for a decrease in frequency. Refer to figure 3.

The following provides information on how to set on- and off-period.

- Setting the on-period

The output on-period is the discharge period when the CF pin is between the peak value oft $V_{H\text{-}CF} = 4$ V (typical) and V_{FB} .

An approximate on-period of the power MOSFET is obtained from the following formula. Refer to figure 2.

$$T_{ON} = C_{CF} \times (V_{H\text{-}CF} - V_{FB})/I_{ON}$$

whereas, $V_{H\text{-}CF} = 4$ V typ.

$I_{ON} = I_{TR} + 250$ µA typ.

$I_{TR} = (E_{IN} \times NB/NP - V_Z)/R_{TR}$

$V_{FB} = 0.7$ V typ. ($I_{FB} \leq 200$ µA)

$V_{FB} = 4$ kΩ $\times I_{FB}$ typ. ($I_{FB} > 200$ µA)

■ Application Notes (continued)

[1] Operation descriptions (continued)

2. Oscillation circuit (continued)

- Setting the on-period (continued)

T_{ON} : On-period
C_{CF} : Value of a capacitor connected to CF pin
V_{FB} : Voltage internally converted from feedback signal I_{FB}
$V_{H\text{-}CF}$: CF upper limit voltage
I_{ON} : On-period discharge current
I_{TR} : Flowing current at TR pin
E_{IN} : Voltage on primary winding
NB : Number of turns in the bias winding
NP : Number of turns in the primary winding
V_Z : Voltage on Zener diode connected to bias winding
R_{TR} : Value of a resistor connected to the TR pin

The power MOSFET is turned off if the voltage at the CLM pin reaches the pulse-by-pulse overcurrent protection threshold voltage (i.e., –200 mV typical) when the overcurrent protection function of the IC is operating.

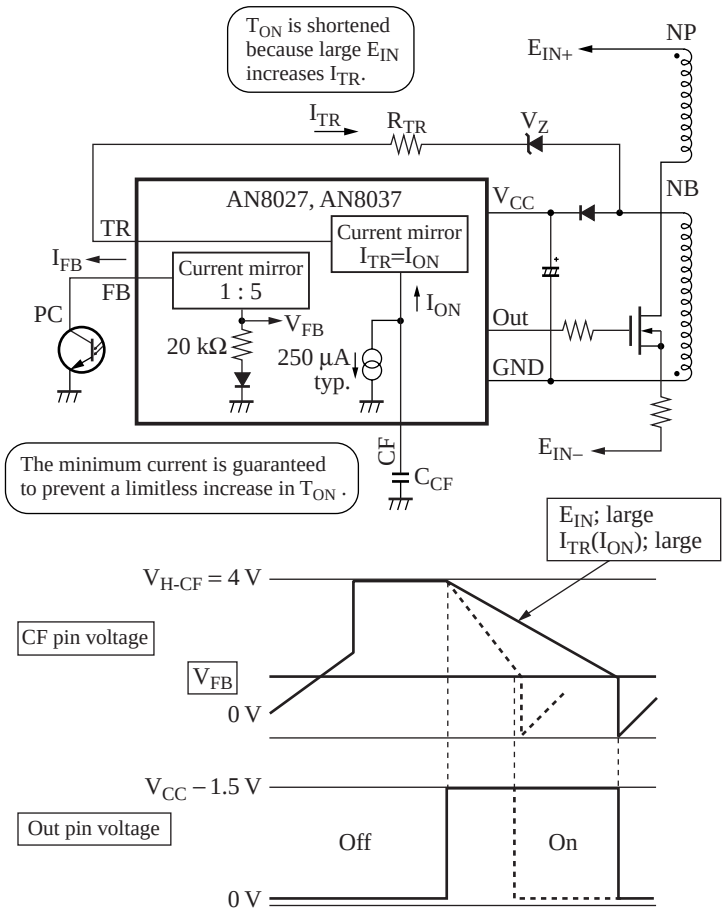


Figure 2. On-period block diagram and control waveform

The maximum on-period can be used for overcurrent protection.
When the input voltage is low, the maximum on-period overcurrent protection is possible.
When the input voltage is high, the CLM pulse-by-pulse overcurrent protection is possible.

■ Application Notes (continued)

[1] Operation descriptions (continued)

2. Oscillation circuit (continued)

- Setting the off-period

The minimum off-period is the charge period from $V_{L\text{-}CF}$ = 0.2 V (typical) to $V_{TH(OFF)}$ or V_{FB} .

An approximate minimum off-period of the power MOSFET is obtained from the following formula. Refer to figure 3.

$$T_{OFF(min)} = C_{CF} \times V_{TH(OFF)} / I_{OFF1} \quad (I_{FB} \leq 0.6 \text{ mA})$$

$$= \{C_{CF} \times V_{TH(OFF)} / I_{OFF1}\} + \{C_{CF} \times (V_{FB} - V_{TH(OFF)}) / I_{OFF2}\} \quad (I_{FB} > 0.6 \text{ mA})$$

$V_{TH(OFF)}$ = 2.4 V typ.

I_{OFF1} = 660 µA typ.

I_{OFF2} = 160 µA typ.

$T_{OFF(min)}$: Minimum off-period

C_{CF} : Value of a capacitor connected to the CF pin

V_{FB} : Voltage internally converted from feedback signal I_{FB}

$V_{TH(OFF)}$: Threshold voltage of V_{FB} to extend off-period

I_{OFF1} : Charge current until CF pin voltage increases from 0.2 V to 2.4 V

I_{OFF2} : Charge current until CF pin voltage increases from 2.4 V to V_{FB}

When the IC is in local resonance operation, the off-period is determined by the longer one of either the time required for the input voltage on the TR pin to drop below the threshold voltage or the minimum off-period ($T_{OFF(min)}$) specified by the C_{CF}.

Thus the power MOSFET is in continuous on/off operation.

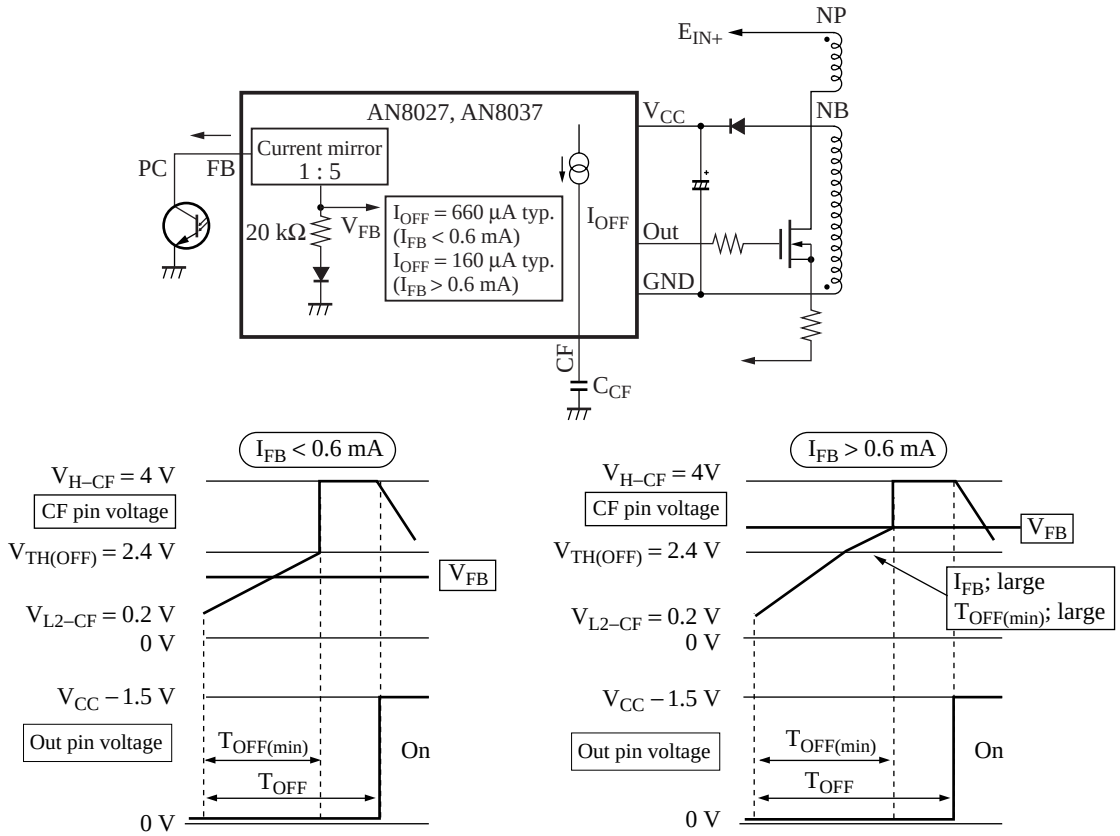


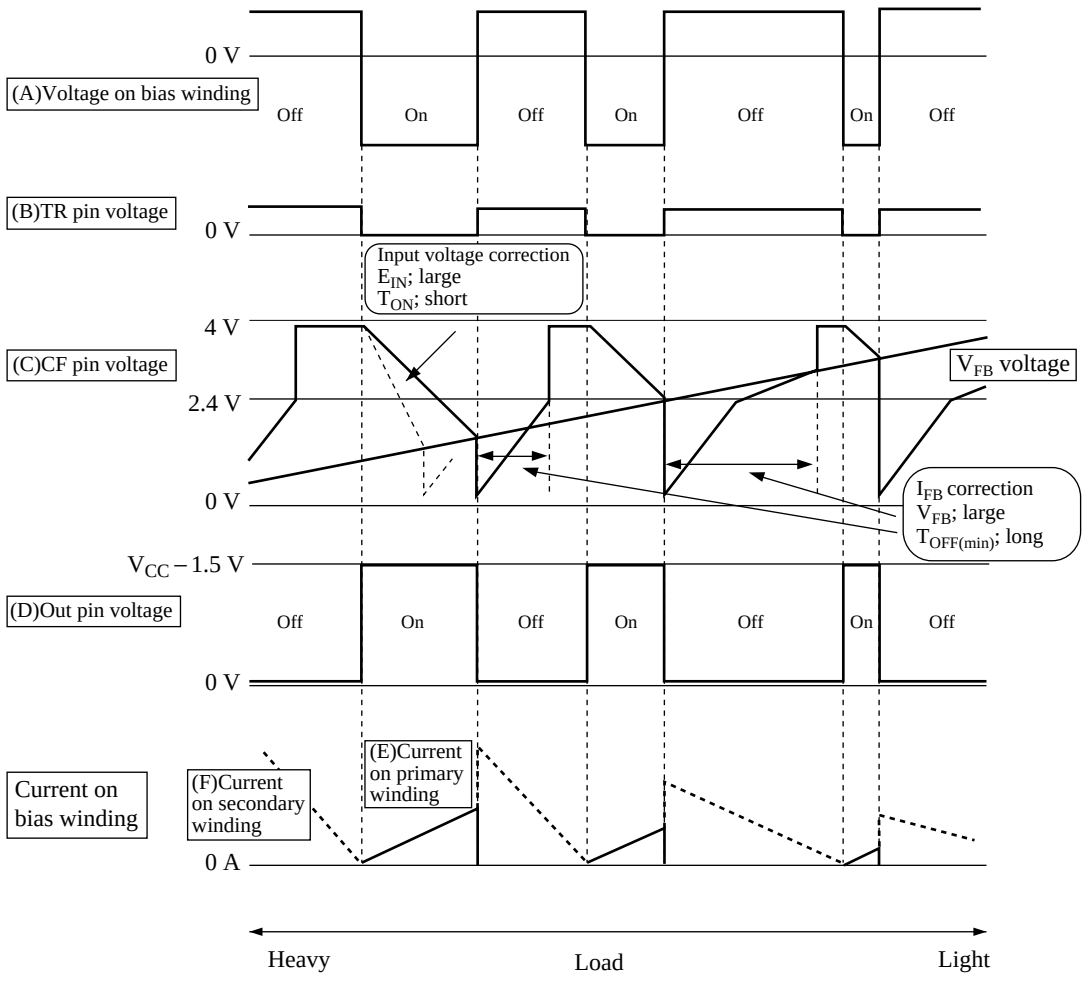
Figure 3. Off-period block diagram and control waveform

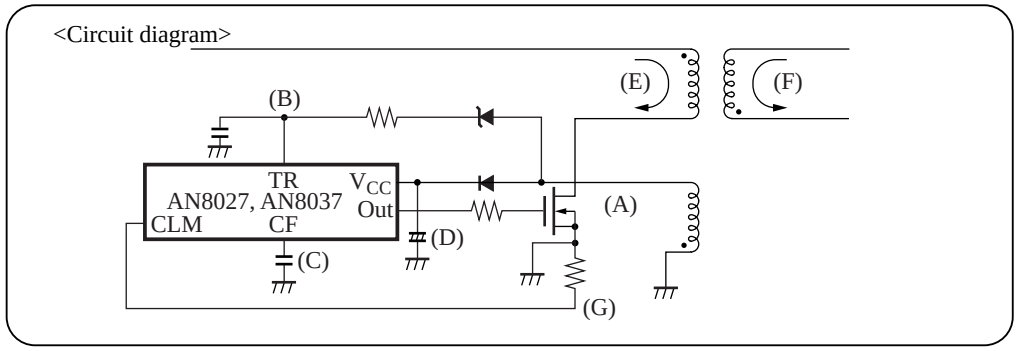
■ Application Notes (continued)

[1] Operation descriptions (continued)

3. Control waveform timing chart

1) Normal (RCC contiuous) operation mode



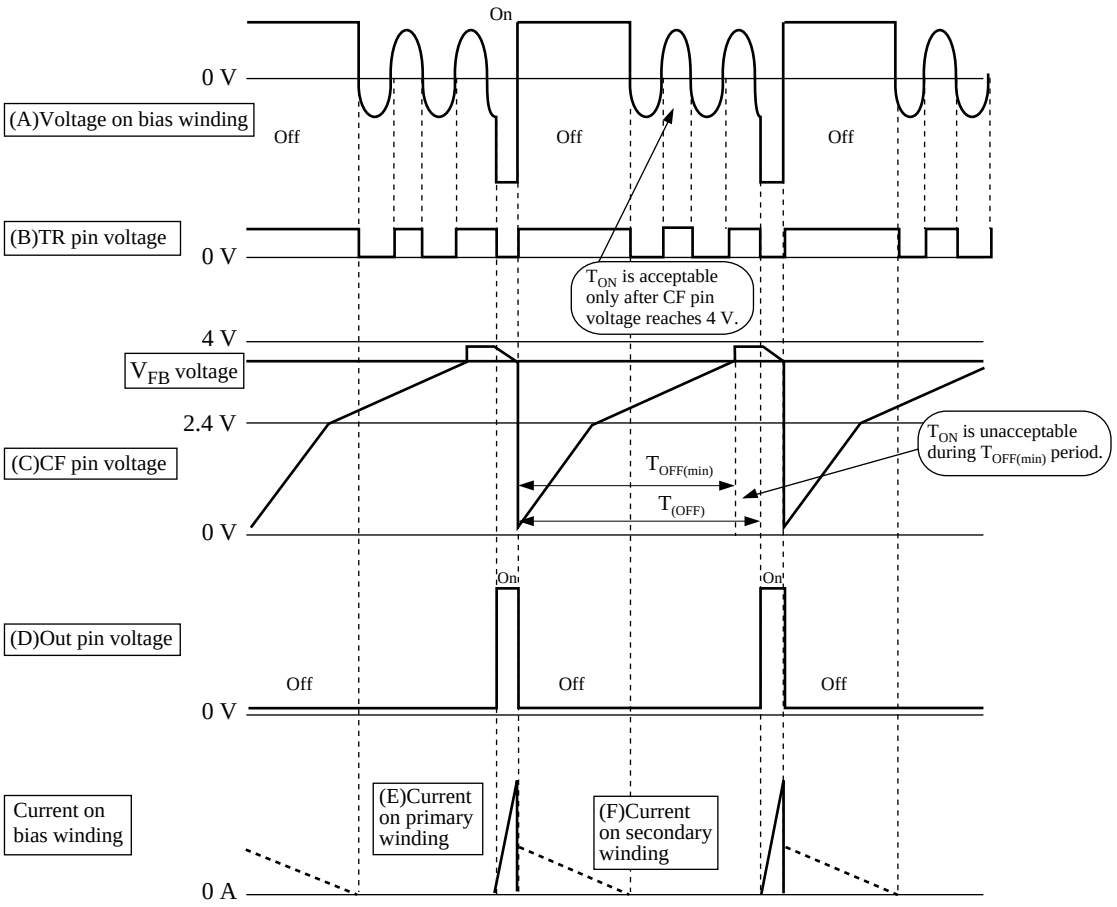


■ Application Notes (continued)

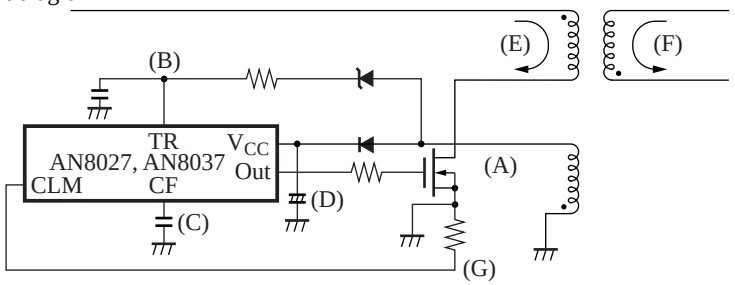
[1] Operation descriptions (continued)

3. Control waveform timing chart (continued)

2) Standby (Intermittent) mode (for light loads)



<Circuit diagram>

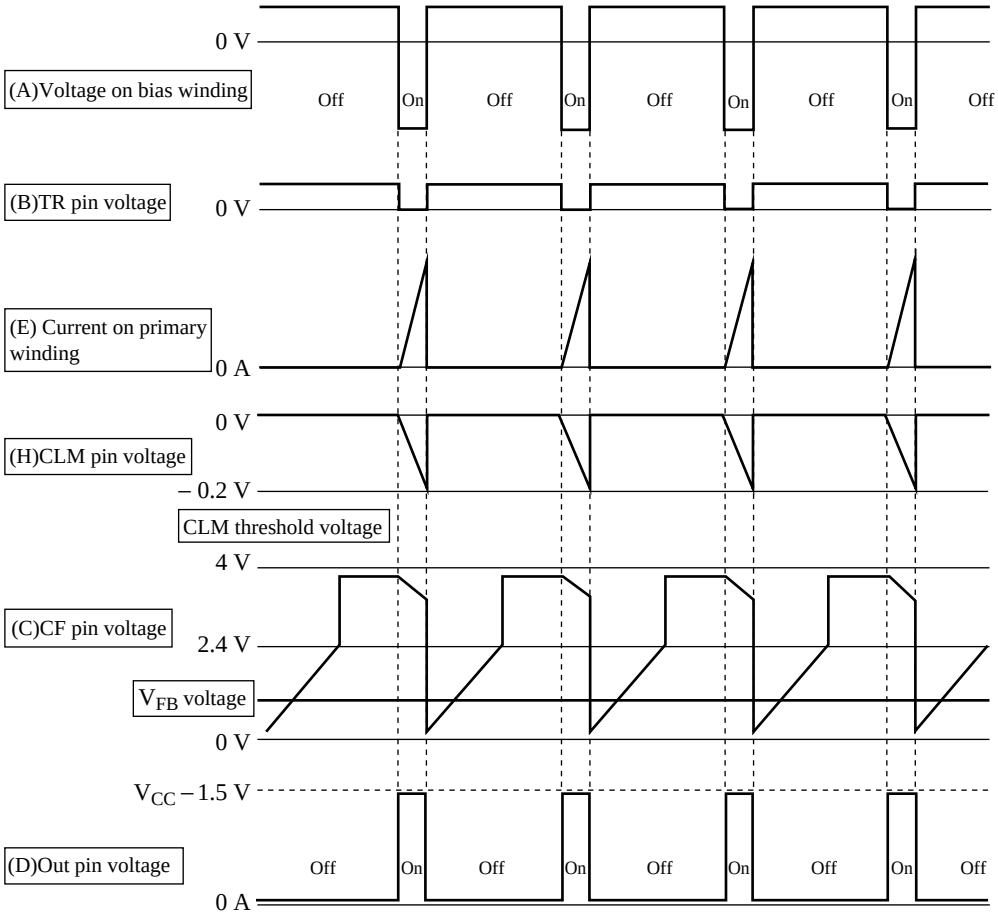


■ Application Notes (continued)

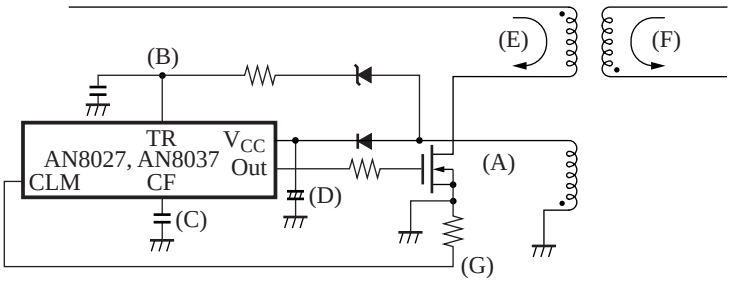
[1] Operation descriptions (continued)

3. Control waveform timing chart (continued)

3) Pulse-by-pulse overcurrent protection (CLM) operation



<Circuit diagram>



■ Application Notes (continued)

[1] Operation descriptions (continued)

4. Power supply output control system (I_{FB}: feedback)

Constant-voltage control of the power supply output is performed by changing the on- and off-period of the power MOSFET. The on- and off-period are controlled with the photocoupler connected to the FB pin (Pin 9). The photocoupler adjusts the current at the FB pin according to the signal that is output from the output voltage detection circuit on the secondary side and changes the V_{FB} voltage. Refer to figure 4.

The higher the AC input voltage is and the lower the load current is, the higher the current flow from FB pin, the higher the V_{FB} voltage, and the shorter the on-period (or longer the off-period in standby mode) will be.

Note that a current cancellation capacity of about 200 μA is provided to compensate for the dark current of the photocoupler. Refer to figure 5.

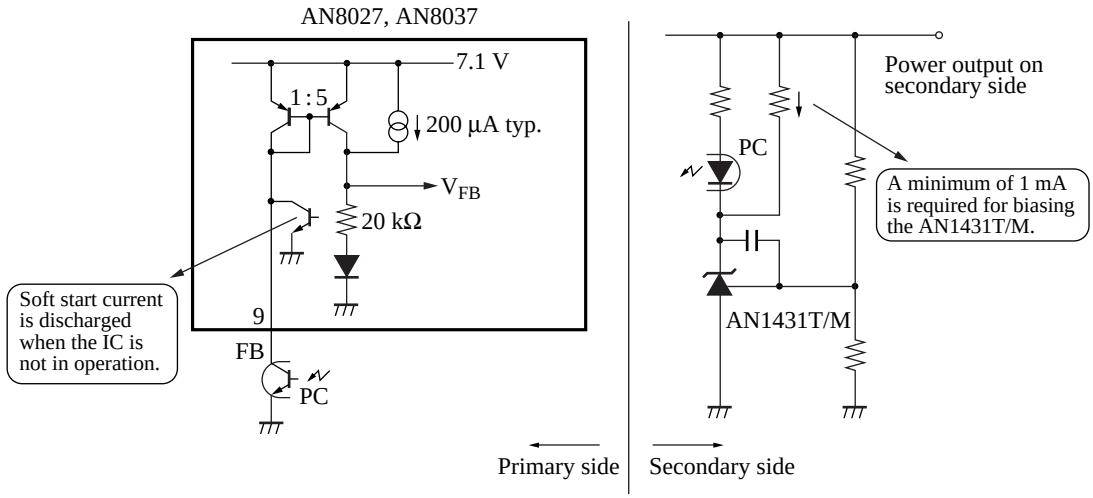


Figure 4. Power output control

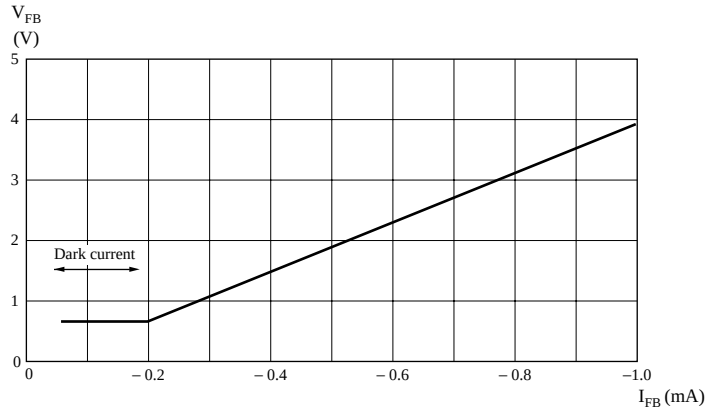


Figure 5. Feedback current vs. V_{FB} characteristics

5. Soft start

When a power supply is started, it starts up in an overload state due to the capacitor connected to the power supply output. At that moment, the output voltage is low. Therefore, the IC in usual voltage regulation tries to start up the power output circuit at a maximum duty cycle. Although the IC tries to limit the current by the pulse-by-pulse overcurrent protection at the CLM pin, the pulses cannot be suppressed to zero due to delays caused by the filter. As a result, high current flows to the main switch (i.e., power MOSFET) and to the diode on the secondary side. Therefore, in the worst case, these components are totally broken. To prevent this, soft start is used to suppress inrush currents at power supply startup.

■ Application Notes (continued)

[1] Operation descriptions (continued)

5. Soft start (continued)

As shown in figure 6, connect R3 and C4 between the FB pin (Pin 9) and GND pin (Pin 5) so that the switching regulator will be in soft start operation. When the voltage supplied to the IC reaches the start voltage and the operation of the startup circuit begins, an open bias voltage of approximately 6.4 V is output to the FB pin. As a result, the charge current I_{FB} flows into C4 from the FB pin. Then the switching regulator starts up at high V_{FB}, thus performing output control while the T_{ON} period is short. The voltage difference between both edges of C4 rises according to the time constant determined by R3 and C4, thus decreasing I_{FB} with the lapse of time and increasing the T_{ON} period gradually.

The above operation increases the flow of current to the power MOSFET gradually after the switching regulator is turned on, thus suppressing the inrush current. However, this reduces the transient response of the feedback loop, so care is required in designing this circuit.

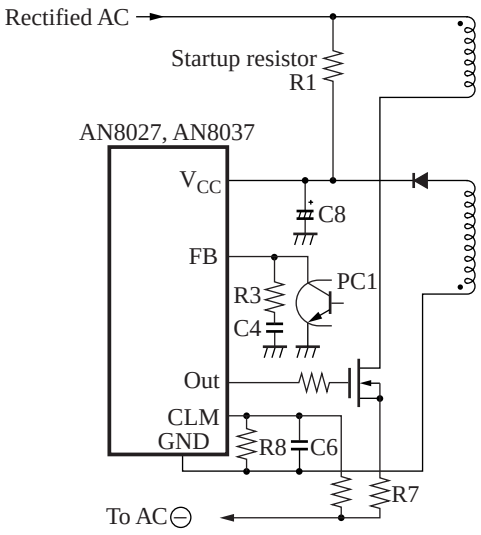


Figure 6

- Notes on selecting R3

The oscillation circuit of this IC is designed under the condition that the T_{ON} period is definite. If excessively low resistance value for R3 is selected, the slope of the triangular wave on the CF pin immediately after the startup may become extremely steep, leading to malfunction of the oscillation circuit. Accordingly, we recommend that you adjust R3 so that the drive pulse width t_1 immediately after the startup is 0.5 ms or greater. (Refer to figure 7.)

Note that the drive pulse width t_1 depends on the capacitance value of the C_{CF} that is connected to the CF pin (Pin 3). Figure 8 indicates recommended values of R3 corresponding to the capacitance value C_{CF}.

(In actual mounting conditions, the correlation shown in figure 8 may deviate slightly.)

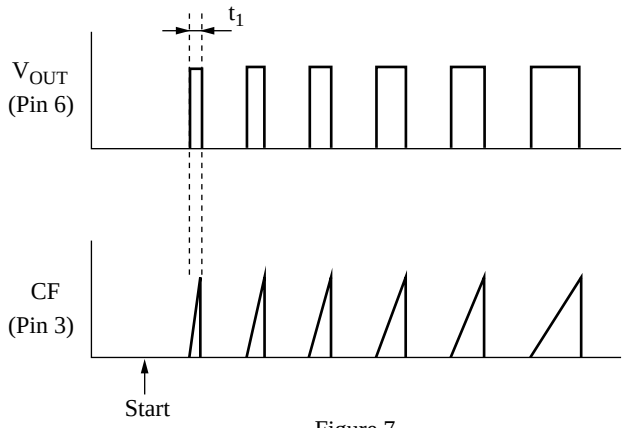


Figure 7

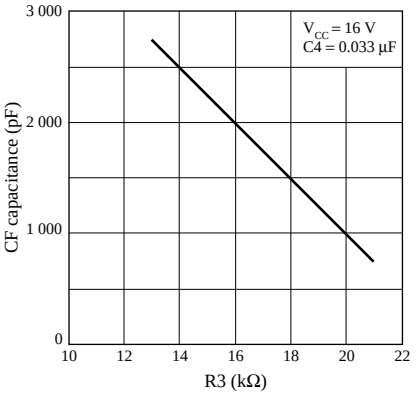


Figure 8

■ Application Notes (continued)

[1] Operation descriptions (continued)

5. Soft start (continued)

- Effective period for the soft start

The effective period for the soft start with the connection of R3 and C4 to the FB pin is approximately calculated by the following formula.

[Approximate formula]

$t_{SS} = R3 \times C4$ (s)

It is thought that the effectiveness of the above formula is weakened because of the following reason:

The voltage difference between both ends of C4 rises up to 63% of the voltage at the FB pin within the time constant τ (= R3 × C4), resulting in decrease of the charge current I_{FB}, although it depends on the value of R3.

Note that if you increase the capacitance value of C4 unnecessarily, it would decrease the sensitivity of the feedback by the photocoupler.

- Soft start at the re-startup

This IC includes a discharge circuit to instantly discharge charged electrons in the capacitor connected to the FB pin in order to ensure the soft start at the re-startup.

Conditions for the operation of the discharge circuit are as follows:

1) V_{CC} has become the stop voltage or below. (at the normal operation)
2) V_{CC} has become the OVP reset threshold voltage or below. (at the OVP operation)

6. Notes on the feedback control

If the IC output pin (pin 6) falls to a negative voltage lower than that of the GND pin, the startup operation may fail or the output oscillation may become unstable.

ICs in general, not just this IC, do not respond well when negative voltages lower than the ground level are applied to their pins. (Except for special applications.) This is because parasitic device operations may be induced when negative voltages are applied due to the structure of ICs themselves.

In the case mentioned above, when the IC output (V_{OUT}) is turned off, the power MOSFET drain-to-source voltage, V_{DS}, jumps from a low voltage to a high voltage. The voltage chattering that occurs at this time is superposed on V_{OUT} through the parasitic capacitance Cgd between the power MOSFET gate and drain, and generates a negative voltage with respect to the pin. No problems occur if the peak voltage, Vex, of this negative voltage does not exceed the parasitic device conduction voltage (about – 0.7 V).

However, the amplitude of the chattering is larger for higher input voltages and for larger leakage inductance in the transformer used. Also, the influence of this phenomenon becomes more noticeable for the larger Cgd of the power MOSFET used, and the Vex peak value also increases. If the parasitic device conduction voltage is exceeded, then, in this IC, the parts of the circuit around the feedback circuit (FB) (in particular, the FB discharge circuit) are influenced. This can cause momentary drops in the FB pin voltage (the control voltage), and as a result increase the FB current I_{FB} and thus does not allow the drive pulse on-period T_{ON} to be increased. It may also prevent stabilization of the circuit. These are symptoms of the case described here. (Refer to figures 9 and 10.)

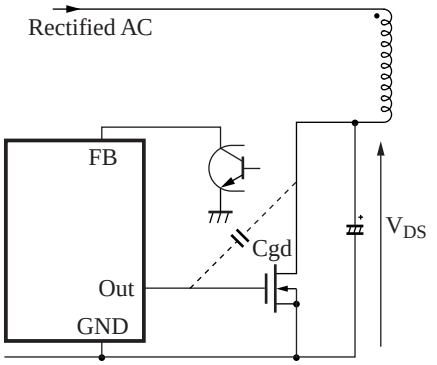


Figure 9

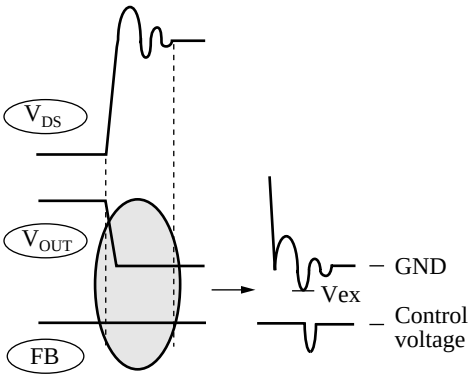


Figure 10

■ Application Notes (continued)

[1] Operation descriptions (continued)

6. Notes on the feedback control (continued)

[Countermeasures]

If an application exhibits the symptoms of the case described above, or similar symptoms, first insert a Schottky barrier diode between V_{OUT} and GND. It is not possible to completely remove the mechanism described above from a power supply system. It is also not possible to prevent levels from being pulled down to negative voltages in the control IC itself. Therefore, the most important point in designing countermeasures is to prevent such negative voltages from reaching the parasitic device conductance voltage.

Note) If a Schottky barrier diode is added to the circuit and the condition improves initially but the symptoms reappear when the input voltage or other parameter is increased, try replacing the Schottky barrier diode with one that has a larger forward current (both peak and average values). The current capacity of the Schottky barrier diode is sometime insufficient.

(Reference)

The following our Schottky diodes are available.

Part No.	Reverse voltage	Forward current (average)	Forward current (peak)
MA2C700A (MA700A*)	30 V	30 mA	150 mA
MA2C723 (MA723*)	30 V	200 mA	300 mA
MA2C719 (MA719*)	40 V	500 mA	1 A

Note) *: Former part number

7. Local resonance operation (power MOSFET turn-on delay circuit)

Local resonance operation by using the AN8027 or AN8037 is possible with circuits as shown in figure 13. C7 is the resonance capacitor, and R9 and C9 form a delay circuit for adjusting the power MOSFET turn on time.

When the power MOSFET is off, the voltage that occurs in the drive winding is input to the TR pin (pin 1) through R9 and C9. The power MOSFET will be held in the off state while a high level (a level higher than the threshold voltage, which is 0.25 V typical) is input to the TR pin.

The TR pin also has a clamping capability for upper and lower limit voltages. The upper limit voltage is clamped at 0.7 V (typical) (sink current: −3 mA), and the lower limit voltage is clamped at about – 0.15 V typical (source current: 3 mA). (Refer to figure 11.)

The power MOSFET off-period is determined by the longer period of the following two periods: the period until the TR pin input voltage becomes lower than the threshold voltage as the bias winding voltage falls after the transformer discharges its energy, and the minimum off-period ($T_{OFF(min)}$) stipulated by the internal oscillator. (Refer to the "Setting the off-period" section in the "Operating descriptions, 2. Oscillation circuit.") As a result, ringing in the bias winding does not be regarded as a turn on signal during the minimum off-period.

■ Application Notes (continued)

[1] Operation descriptions (continued)

7. Local resonance operation (power MOSFET turn-on delay circuit) (continued)

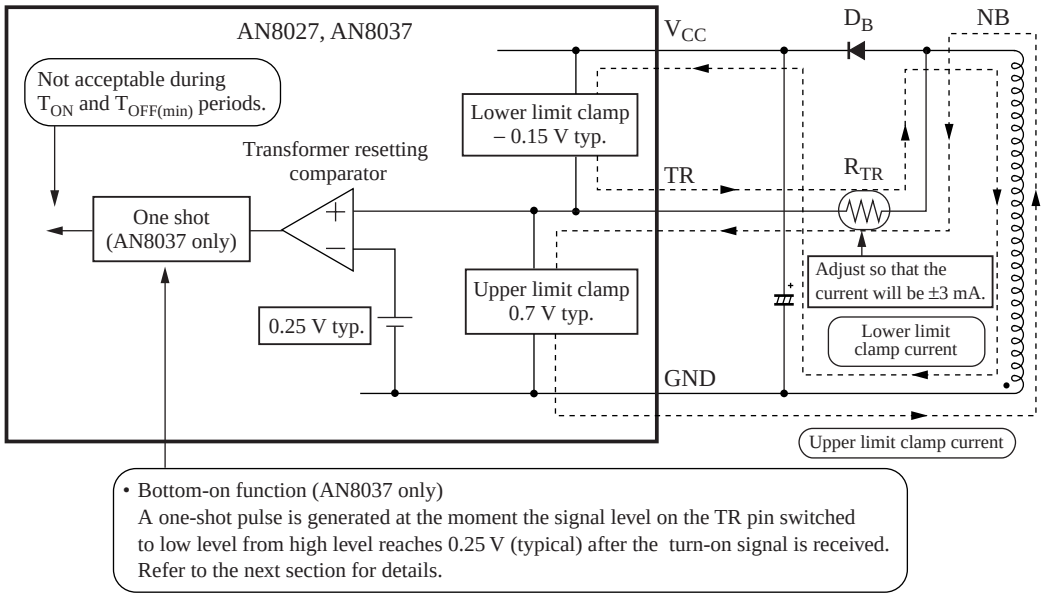


Figure 11

8. Bottom-on function (AN8037 only)

Unlike the AN8027 or our conventional AN8026, AN8028, or AN8029 IC, which detects transformer resetting with the high or low level in comparison to the threshold voltage on the TR pin, the AN8037 detects transformer resetting on the falling edge across the threshold voltage.

This ensures the reliable local resonance operation of the IC regardless of input voltage fluctuations in a wide input range for worldwide use, thus eliminating difficulty in turning on the power MOSFET when V_{DS} is close to the minimum value. Refer to figure 12.

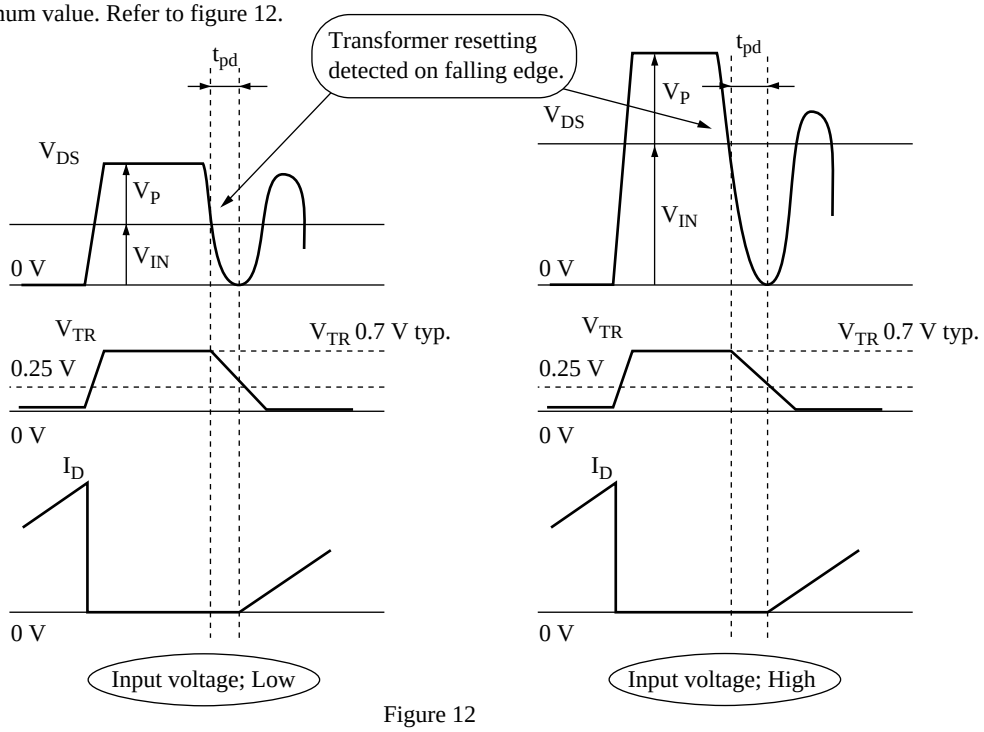


Figure 12

■ Application Notes (continued)

[1] Operation descriptions (continued)

8. Bottom-on function (AN8037 only) (continued)

Select the constants of R9 and C9 to determine the turn-on delay time so that the power MOSFET will be turned on at a frequency of half the resonant frequency. Practically, refer to figure 12 and determine the turn-on delay time so that the power MOSFET will be turned on at $V_{DS} = 0$ V. The approximate resonant frequency can be obtained from the following formula.

$$f_{SYNC} = \frac{1}{2\pi\sqrt{L \cdot C}} \text{ [Hz]}$$

C: resonant capacitance

L: inductance of primary winding of transformer

The turn-on delay time $t_{pd(ON)}$ to turn on the power MOSFET at a frequency of half the resonant frequency is, therefore, as follows.

$$t_{pd(ON)} = \pi\sqrt{L \cdot C} \text{ [s]}$$

Note that since insertion of the resonance capacitor results in increased losses, using the parasitic capacitance of the power MOSFET itself should also be considered. However, in this case the sample-to-sample variations and temperature variations should be considered.

9. Notes on R9 and C9 value selection

If an excessively low value is used for R9, the current flowing into the TR pin after power supply startup will exceed the maximum rating for the IC, and incorrect operation (in the worst case, destruction of the device) may occur. We recommend using a value of R9 in the range that satisfies the following conditions.

$$\frac{V_{B(-)} - \text{The TR lower limit clamp voltage } (-0.15 \text{ V typical})}{R9} \geq -3 \text{ mA}$$

$V_{B(-)}$: negative peak voltage

$$\frac{V_{B(+)} - \text{The TR upper limit clamp voltage } (1.5 \text{ V typical})}{R9} \leq 3 \text{ mA}$$

$V_{B(+)}$: positive peak voltage

Adjust $t_{PD(ON)}$ with C9 by taking the inductance and resonant capacitance of the transformer into consideration.

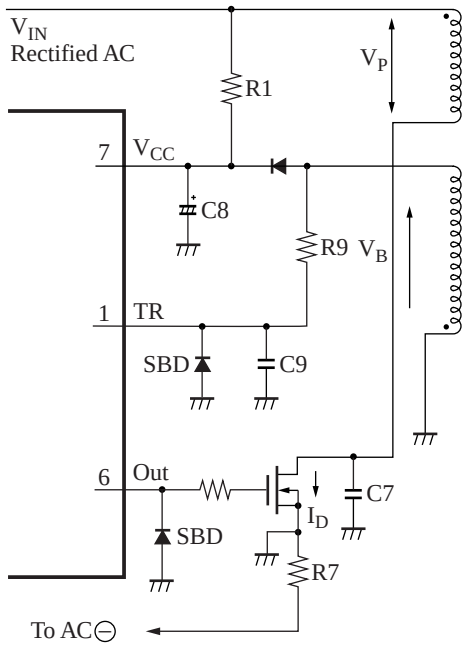


Figure 13

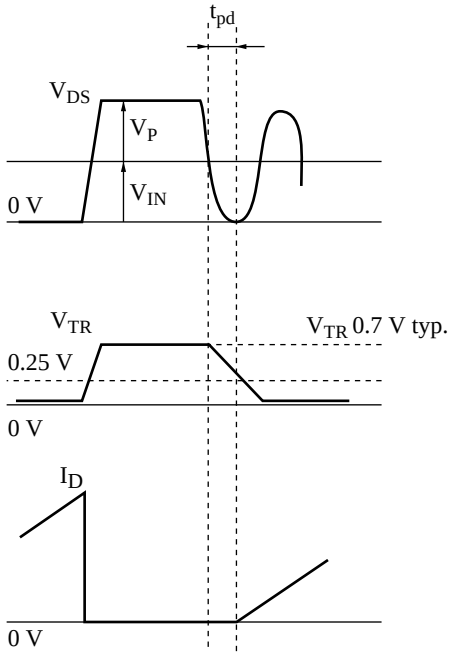


Figure 14

■ Application Notes (continued)

[1] Operation descriptions (continued)

10. Output block

This IC adopts a totem pole (push-pull) structure output circuit in which NPN transistors as shown in figure 15 sinks and sources current to rapidly drive the power MOSFET which is a capacitive load.

This circuit provides maximum sink and source currents of ±0.1 A (DC), and peak currents of ±1.0 A. Furthermore, this circuit has a sink capability of 1 mA (typical) even when the supply voltage has fallen under the stop voltage, and thus can turn off the power MOSFET reliably.

The main requirement on the control IC in this type of power supply is the ability to provide a large peak current. That is to say, a high average current is not required in steady state operation. This is because the power MOSFET is a capacitive load, and while a large peak current is required to drive such a load rapidly, once the load has been charged or discharged a much smaller current suffices to retain that state.

This IC has a guaranteed peak current capability of ±1 A, values which were determined by considering the capacitance of the power MOSFETs that will be used.

The parasitic inductance and capacitance of the power MOSFET can cause ringing, and pull down the output pin below the ground level. If the output pin goes to a negative voltage that is larger than the voltage drop of the diode, this state can turn on the parasitic diode formed by the collector of the output NPN transistor and the substrate. Insert a Schottky barrier diode between the output and ground if this is a problem. (Refer to figure 15.)

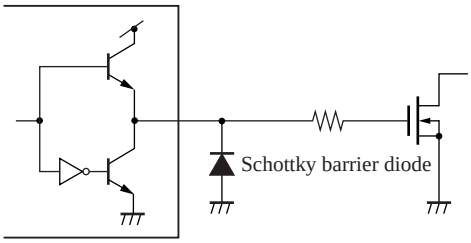


Figure 15

11. Timer latch

The pulse-by-pulse overcurrent protection function by itself cannot fully protect the transformer, the first recovery diode or Schottky diode on the secondary side, or the power MOSFET, if the power output is overloaded or short-circuited for a certain period. If the overcurrent state continues for a certain period or longer time, the timer latch function makes it possible to interrupt the IC in a certain period by charging the capacitor connected to the SD pin.

The overload of the power output or short-circuiting of the power output is monitored as a voltage drop in power output, at which time the pulse-by-pulse overcurrent protection is in operation. The voltage drop in power output is detected as a decrease in current through the FB current feedback pin (pin 9). If this current is less than a certain value, the on-chip comparator of the IC is in inverted operation to provide constant current to the SD pin. Refer to figure 16.

Then external capacitor connected to the SD pin is charged and the voltage on the SD pin rises to the SD operating threshold voltage (i.e., 3.9 V typical), overvoltage protection (OVP) is triggered, and the operation of the IC is suspended. Refer to figure 17.

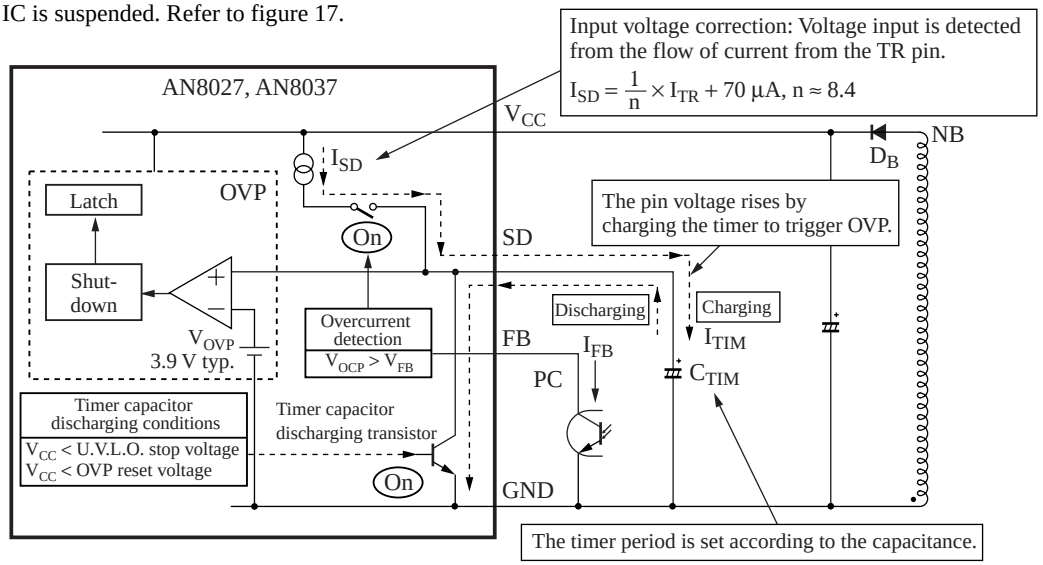


Figure 16

■ Application Notes (continued)

[1] Operation descriptions (continued)

11. Timer latch (continued)

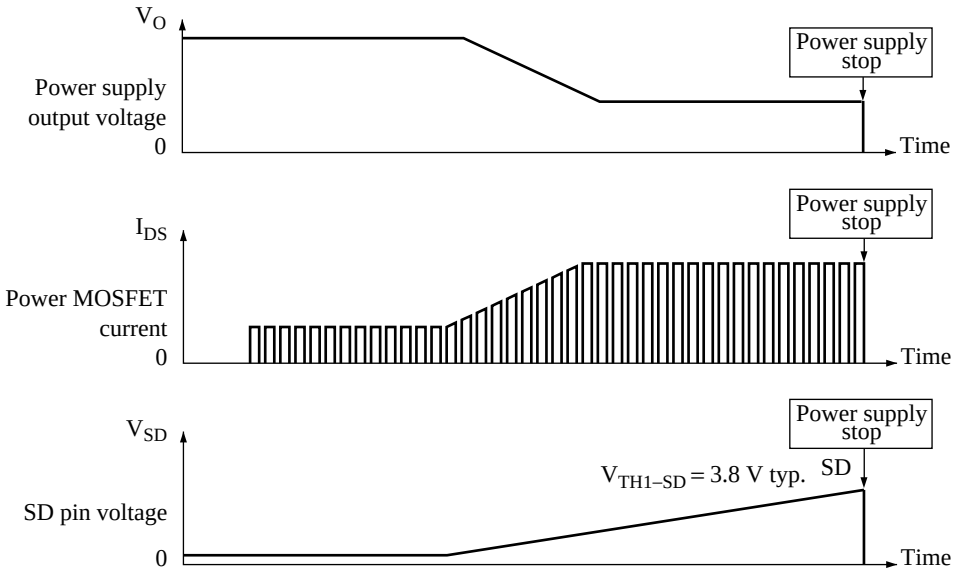


Figure 17. Basic timer latch operation

12. Setting the timer period

The period between the detection of the erroneous power output and the moment OVP is triggered (hereinafter called timer period) needs to be longer than the rise time of the power supply. Since at operation start the IC is in the same condition as the overload or output short-circuit condition, if the timer period is shorter, the power supply works latch and can not start.

Therefore, the IC has a design making it possible to adjust the timer period with the external capacitor connected to the SD pin. Make sure, however, that the capacitor is not too high, otherwise the power supply may be damaged.

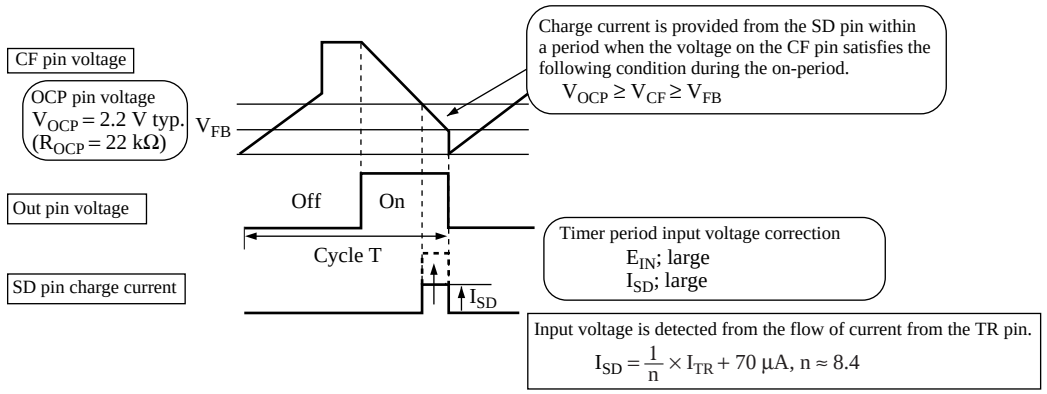


Figure 18

■ Application Notes (continued)

[1] Operation descriptions (continued)

12. Setting the timer period (continued)

Timer period (T_{TIM}) is obtained from the following formula.

$T_{TIM(S)} = \{C_{SD} \times (V_{TH1\text{-}SD} - V_{STB\text{-}SD})\}/I_{SD(AVE)}$

$V_{TH1\text{-}SD} = 3.9$ V typ.
$V_{STB\text{-}SD} = 1.6$ V typ.
$I_{SD(AVE)} = I_{SD} \times T_{SD}\ /T$
$T_{SD} = C_{CF} \times (V_{OCP} - V_{FB})/I_{ON}$
$T_{SD} = C_{CF} \times (V_{OCP} - V_{FB})/I_{ON}$

C_{SD} : Capacitor connected to SD pin
$V_{TH1\text{-}SD}$: Shutdown operating threshold voltage 3.9 V typ.
$V_{STB\text{-}SD}$: Shutdown standby voltage 1.5 V typ.
I_{SD} : Timer latch charge current
T_{SD} : Timer latch charge period
T : Cycle
C_{CF} : Capacitor connected to CF pin
V_{OCP} : OCP pin voltage = $R_{OCP} \times 100$ µA typ.
V_{FB} : Voltage internally converted from feedback signal I_{FB}

$$= \frac{I_{FB}}{5} \times 20\ k\Omega + V_{BE}$$

I_{ON} : On-period charge current = 250 µA typ. $\times \frac{I_{TR}}{4}$

By detecting the overload level on the secondary side from I_{FB} and changing T_{SD} , the timer period can be adjusted according to the overload level. Furthermore, in the application circuit, the timer period can be adjusted in both standby and normal modes. To enable this, let the microcomputer on the secondary side detect the operating mode (i.e., either the standby or normal mode) of the IC to vary the value of the resistor connected to the OCP pin with the photocoupler. Refer to figures 19 and 20.

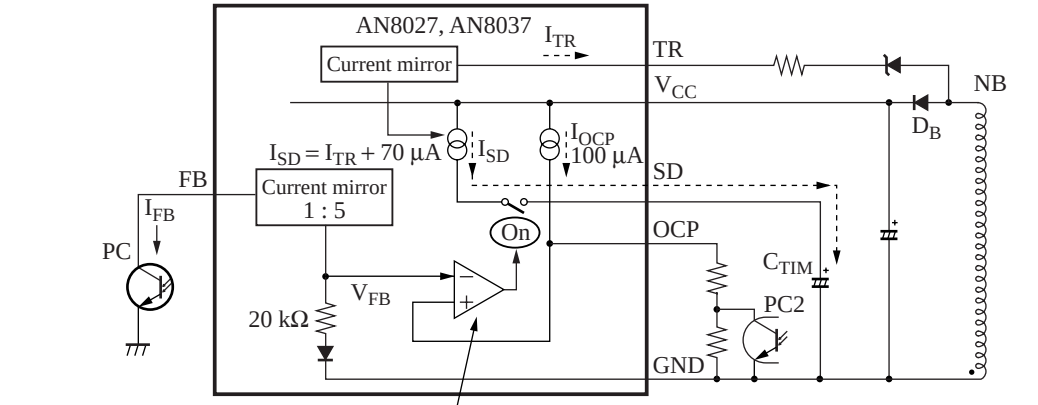


Figure 19

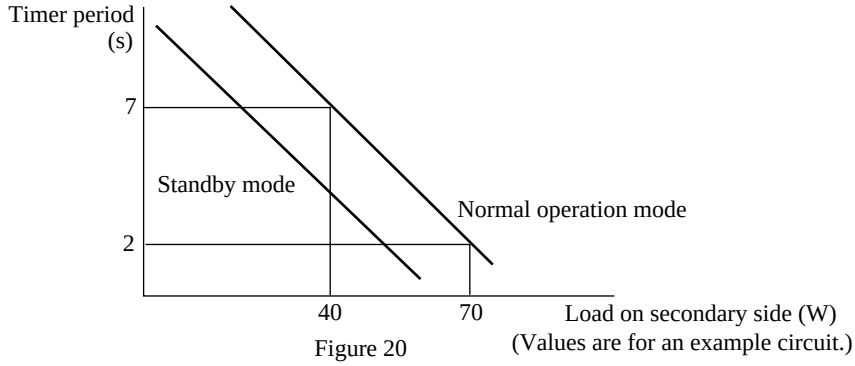


Figure 20

■ Application Notes (continued)

[1] Operation descriptions (continued)

13. Overvoltage protection (OVP) circuit

OVP stands for overvoltage protection. The overvoltage protection circuit is a self-diagnostic function that shuts down the power supply to protect the load if a voltage that is significantly and abnormally higher than the normal output voltage occurs in the power supply output, due to, for example, a malfunction in the control system or an abnormal voltage applied externally. (Refer to figure 22.)

Basically, the overvoltage protection circuit should be designed so that the V_{CC} pin voltage of the IC can be monitored. Since the V_{CC} pin voltage is normally supplied from the transformer bias winding, this voltage is proportional to the secondary side output voltage. Thus the overvoltage protection circuit operates when an overvoltage occurs in the secondary side output.

1) If, as a result of an abnormality in the power supply output, the voltage input to the V_{CC} pin exceeds the threshold value (20.5 V typical), the IC internal reference voltage is shut down, and all control operation is stopped. The IC then holds this state. If latching at a voltage lower than the threshold value is required, connect a Zener diode between the V_{CC} and SD pins as shown in figure 22 and take method 2) below to set the voltage.
2) If the SD pin input voltage exceeds a threshold value of 3.9 V typical, the IC internal reference voltage is shut down, and all control operation is stopped. The IC then holds this state.
3) OVP is reset in two methods. One is to decrease the output voltage on the secondary side so that the V_{CC} pin voltage is less than the OVP reset voltage, i.e., 8.1 V typical. The other is to decrease the SD pin input voltage (V_{SD}) to a value less than the SD reset voltage, i.e., 0.7 V typical, by external resetting. If V_{SD} is less than 0.1 V typical, however, the IC will be in remote operation to shut off the output.
The IC incorporates a circuit that discharges a constant current of approximately 25 mA from the capacitor connected to the SD pin for the re-start operation. The operation of this circuit is stopped when the SD pin voltage drops to 1.5 V or below. Refer to figure 21.

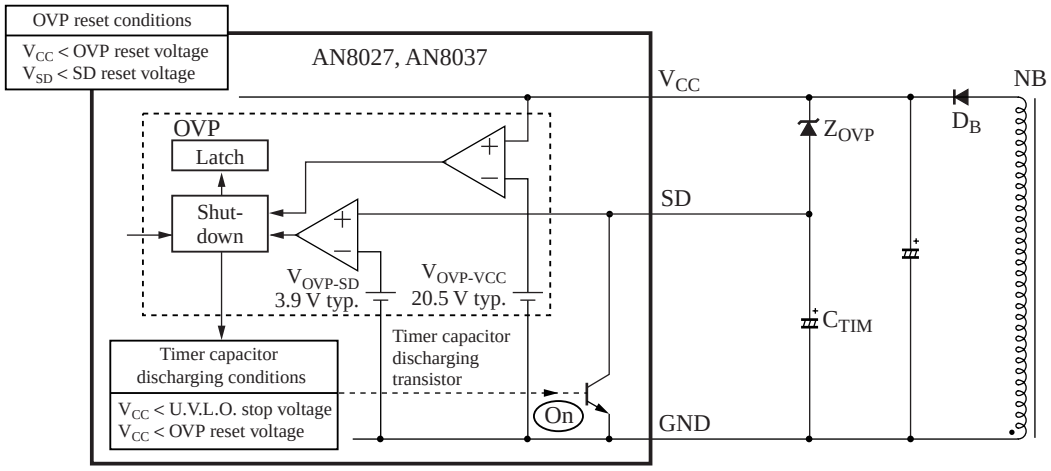


Figure 21

The following is a formula to allow the IC to be in OVP operation with the SD pin in the above method 2).

$$V_{th(OUT)} = \frac{V_{(OUT)}\ \text{Secondary side output voltage under normal operation}}{V_{CC}\ \text{pin voltage under normal operation}} \times V7$$

$$V7 = V_{TH\text{-}SD1} + V_Z$$

$V_{th(OUT)}$: Secondary side output overvoltage threshold value
$V_{TH\text{-}SD1}$: SD operating threshold value
V_Z : Zener voltage (externally connected to OVP pin)

■ Application Notes (continued)

[1] Operation descriptions (continued)

13. Overvoltage protection (OVP) circuit (continued)

- Operating supply current characteristics

When the OVP circuit operates and the power supply current drops, this can induce a rise of the supply voltage V_{CC} . In the worst case, it may exceed the IC's guaranteed breakdown voltage (24 V).

Therefore, the circuit is provided with characteristics that cause the supply current to rise in constant resistance mode when the OVP circuit operates, and thus prevent increases in the supply voltage.

Due to these characteristics, if the supply voltage V_{CC} when the OVP circuit operates is stabilized at a value (note that this value depends on the value of the startup resistor) that is larger than the OVP release voltage, the OVP circuit will not be reset as long as the AC input is not cut. (Refer to figure 23.) Note that this does not apply to an external reset.

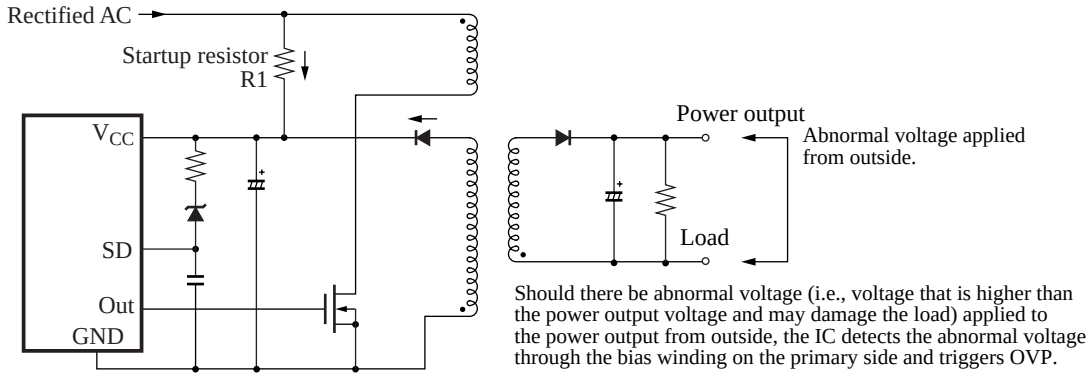


Figure 22

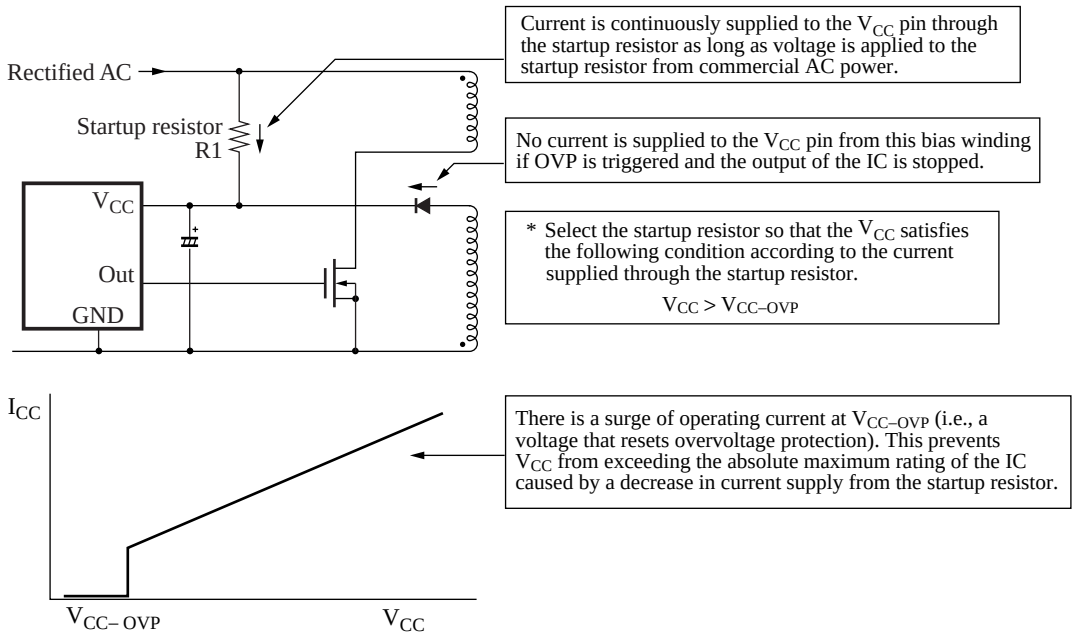


Figure 23

■ Application Notes (continued)

[1] Operation descriptions (continued)

14. Remote on/off function

The SD pin of the AN8027 or AN8037 has a remote on/off function besides the following functions.

- Timer latch function
- Overvoltage protection function

The remote on/off function turns the power supply output on and off remotely with external signals. Furthermore, this function turns the power supply off by setting the SD pin voltage extremely close to the ground voltage (i.e., 0 V) if the capacitor connected to the SD pin for timer latch use is damaged in the short-circuit mode. Refer to figure 24.

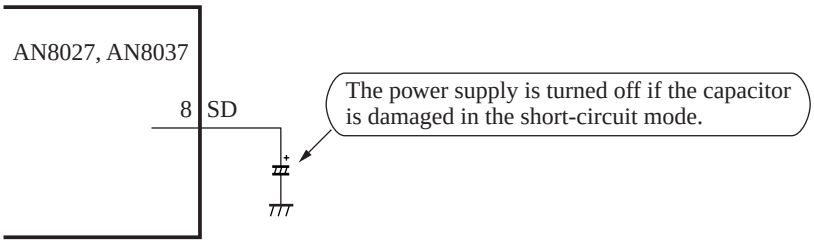


Figure 24

On the other hand, a hysteresis width of 50 mV (typical) is provided for threshold SD voltage to prevent the output of the IC in remote operation from chattering. Refer to figure 25.

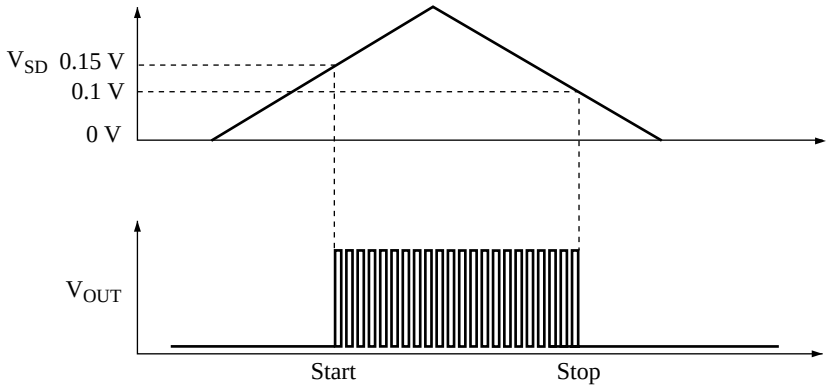


Figure 25

■ Application Notes (continued)

[1] Operation descriptions (continued)

15. Overcurrent protection circuit (pulse-by-pulse overcurrent protection)

This circuit uses the fact that overcurrents in the power supply output are proportional to the current flowing in the primary side main switch (power MOSFET). This circuit limits overcurrents in the power supply output by constraining the upper limit of the pulse current flowing in the main switch, and thus protects components sensitive to excessive current.

The current flowing in the main switch is detected by connecting a resistor between the power MOSFET source and ground and monitoring the voltage that appears across that resistor. When the power MOSFET is turned on and the CLM (current limit) threshold voltage is detected, the output is turned off. This controls the circuit so that a current in excess of that limit cannot flow by turning off the power MOSFET. The CLM threshold voltage is about – 0.2 V typical with respect to ground at T_a = 25°C. While this control operation is repeated every cycle, once an overcurrent is detected, the off state is held for the remainder of that cycle, and the circuit is not turned on until the next period. This type of overcurrent detection is called "pulse-by-pulse overcurrent detection."

R6 and C6 in figure 26 form a filter circuit that rejects noise generated due to the incidental equivalent parasitic capacitance when the power MOSFET is on.

For the grounding point, we recommend that the power MOSFET source pin and the IC GND pin be connected over as short a distance as possible.

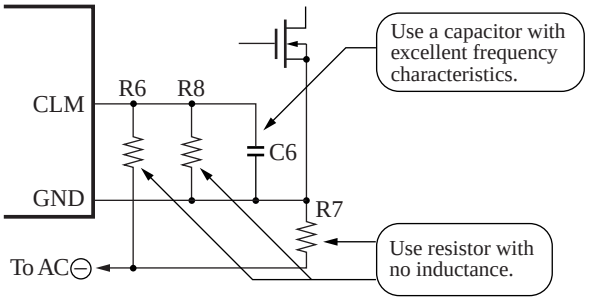


Figure 26

- Notes on the detection level precision

This overcurrent detection level is reflected on the operating current level of the power supply overcurrent protection function. Therefore, if this detection level varies with sample-to-sample variations or with temperature, the operating current level of the overcurrent protection function of the power supply itself will vary. Since variations in this level imply a need for increased ruggedness in parts used, or even the destruction of circuit components, we have increased the precision of this IC as much as possible.

16. Overcurrent protection circuit (input voltage correction function)

As an extended application, this section presents a circuit design that applies a correction so that the overcurrent protection operating point is held fixed with respect to variations in the input voltage. This circuit uses the proportional relationship between the input voltage and the inverted voltage of the bias winding, and superposes inverted voltage of the bias winding on the overcurrent protection operating voltage. (Refer to figures 27 and 28.)

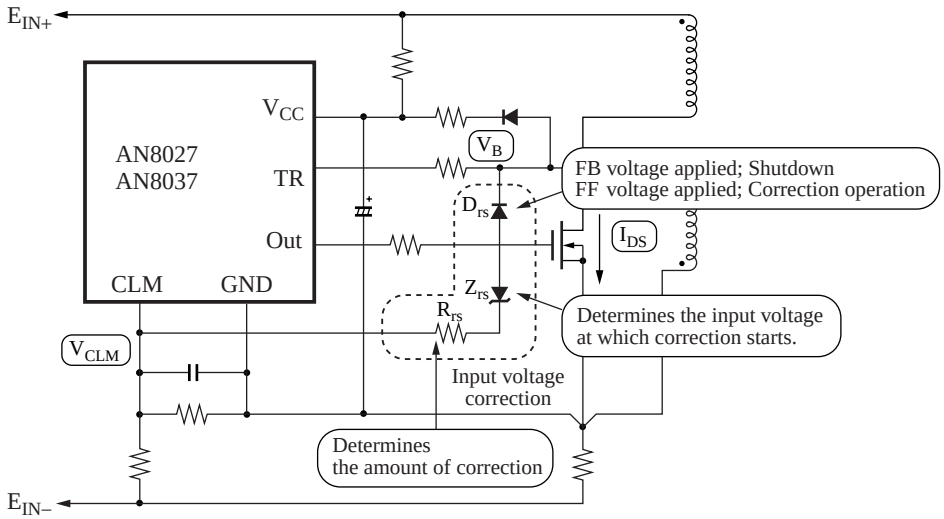


Figure 27

■ Application Notes (continued)

[1] Operation descriptions (continued)

16. Overcurrent protection circuit (input voltage correction function) (continued)

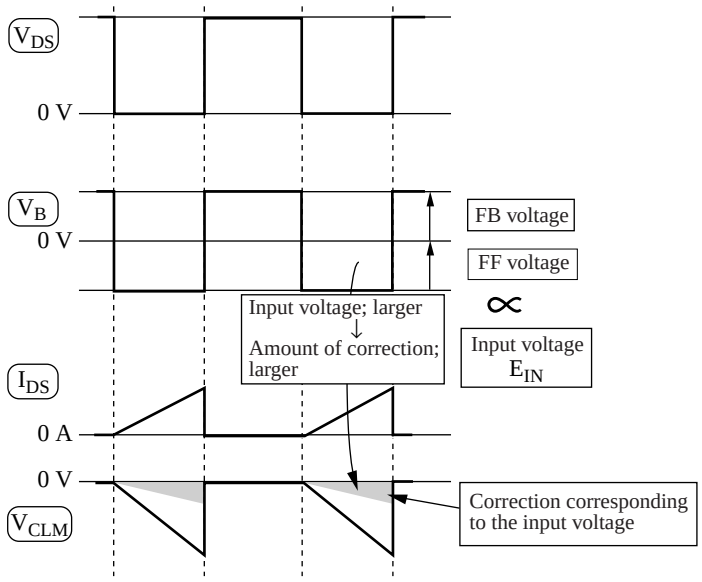


Figure 28

17. Overcurrent protection circuit (Timer latch protection)

The CLM pin is used for timer latch in addition to pulse-by-pulse overcurrent protection.

This is because the pulse-by-pulse overcurrent protection alone cannot prevent the power MOSFET connected to the Out pin from damage in most cases if the primary winding is short-circuited and excessive current flows to the power MOSFET.

If an excessive current flows to the power MOSFET for a certain period due to the short-circuiting of the primary winding, this circuit charges the capacitor connected to the SD pin, shut down the power supply, and holds this state. (Refer to figure 29.)

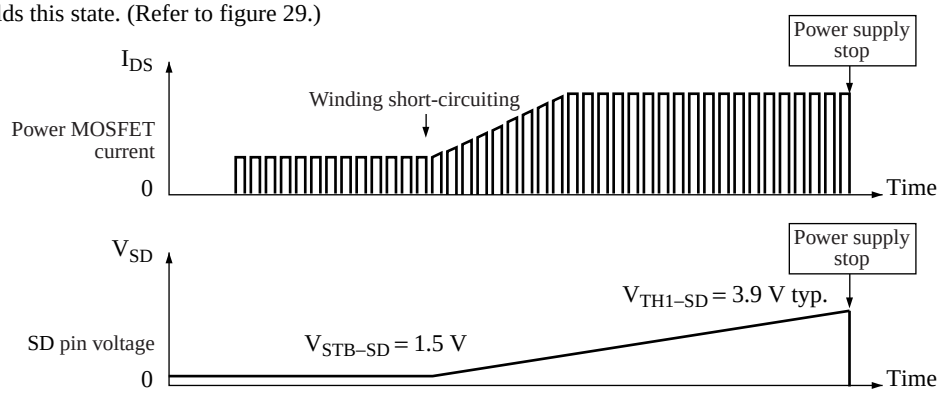


Figure 29

[Setting the timer period]

The timer period (T_{CLM}) is obtained from the following formula.

$T_{CLM} = \{C_{SD} \times (V_{TH1\text{-}SD} - V_{STB\text{-}SD})\}/I_{CLM(AVE)}$

$I_{CLM(AVE)} = I_{CLM} \times T_{OFF} / T$

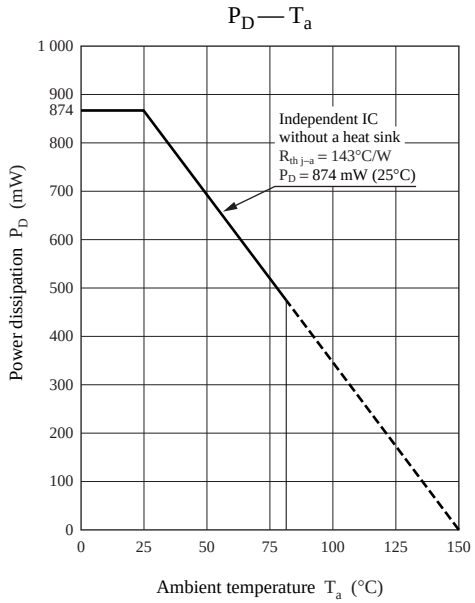
(I_{CLM} = 100 μA)

Example: If T_{OFF} / T is 50%, C_{SD} is 10 μF.
$T_{IM} \approx$ 500 ms

C_{SD} : Capacitor connected to SD pin
$V_{TH1\text{-}SD}$: Shutdown operating threshold voltage
$V_{STB\text{-}SD}$: Shutdown standby voltage
I_{CLM} : CLM timer charge current (100 μA)
T_{OFF} : Off-period
T : Cycle

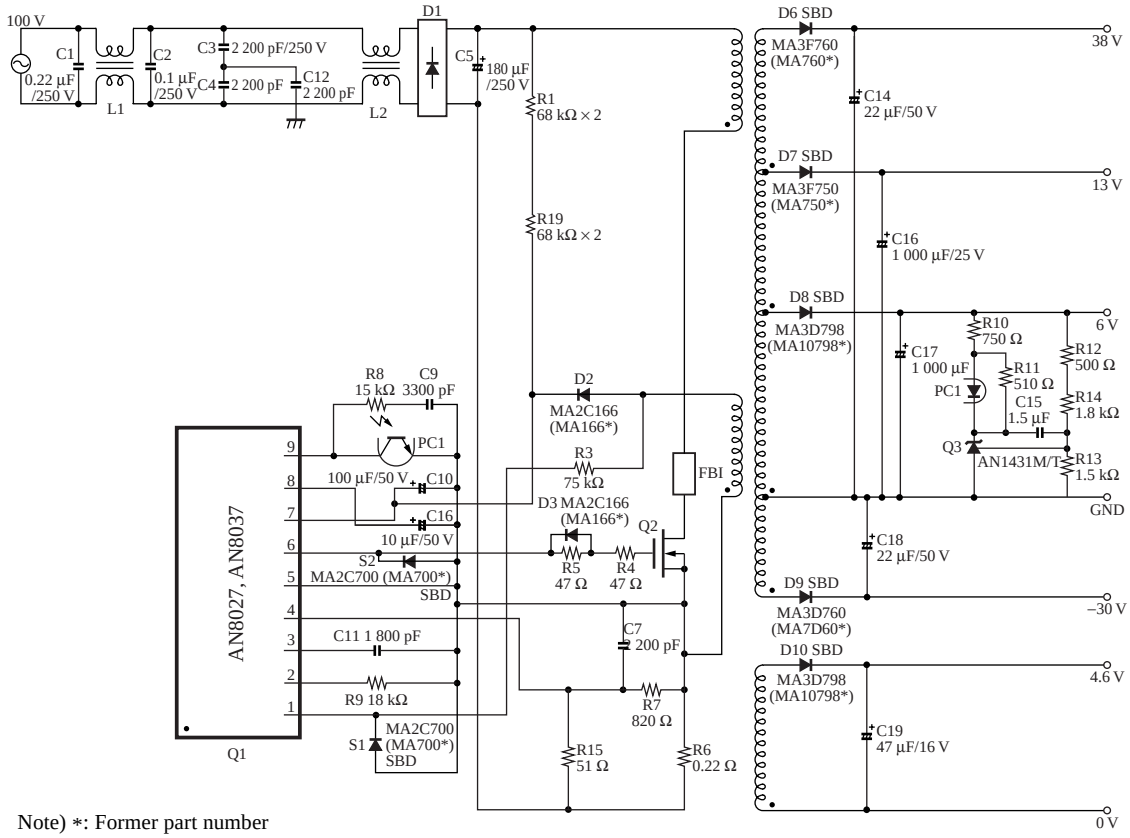
■ Application Notes (continued)

[2] Package power dissipation



■ Application Circuit Examples

• Circuit Diagram



Note) ∗: Former part number

■ Application Circuit Examples (continued)

• Evaluation board chart