

Silicon NPN Power Transistors

2SD1294

DESCRIPTION

- With TO-3P(I) package
- Wide area of safe operation
- High DC current gain
- Darlington

APPLICATIONS

- Power regulator for line operated TV

PINNING

PIN	DESCRIPTION
1	Base
2	Collector;connected to mounting base
3	Emitter

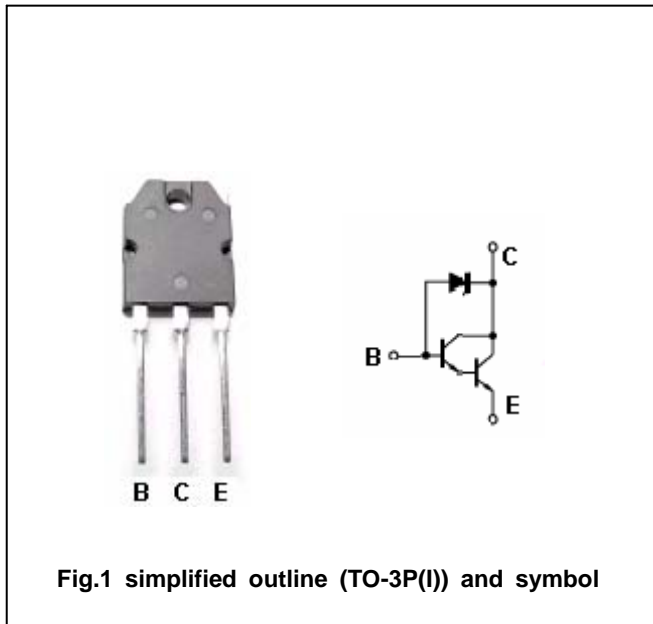


Fig.1 simplified outline (TO-3P(I)) and symbol

Absolute maximum ratings (Ta=25)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	60 ± 15	V
V_{CEO}	Collector-emitter voltage	Open base	60 ± 15	V
V_{EBO}	Emitter-base voltage	Open collector	6	V
I_C	Collector current (DC)		5	A
I_{CP}	Collector current (Pulse)		20	A
P_C	Collector power dissipation	$T_C=25$	80	W
T_j	Junction temperature		150	
T_{stg}	Storage temperature		-55~150	

Silicon NPN Power Transistors

2SD1294

CHARACTERISTICS

T_j=25 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{CEO}	Collector-emitter breakdown voltage	I _C =100mA ; I _B =0	45		75	V
V _{CBO}	Collector-base breakdown voltage	I _C =100mA ; I _E =0	45		75	V
V _{CEsat-1}	Collector-emitter saturation voltage	I _C =0.5A ; I _B =1mA			1.5	V
V _{CEsat-2}	Collector-emitter saturation voltage	I _C =1A ; I _B =1mA			2.5	V
V _{BE}	Base-emitter on voltage	I _C =0.5A ; V _{CE} =5V			1.8	V
I _{EBO}	Emitter cut-off current	V _{EB} =6V ; I _C =0			0.1	mA
h _{FE}	DC current gain	I _C =0.5A ; V _{CE} =5V	2000		20000	

Silicon NPN Power Transistors

2SD1294

PACKAGE OUTLINE

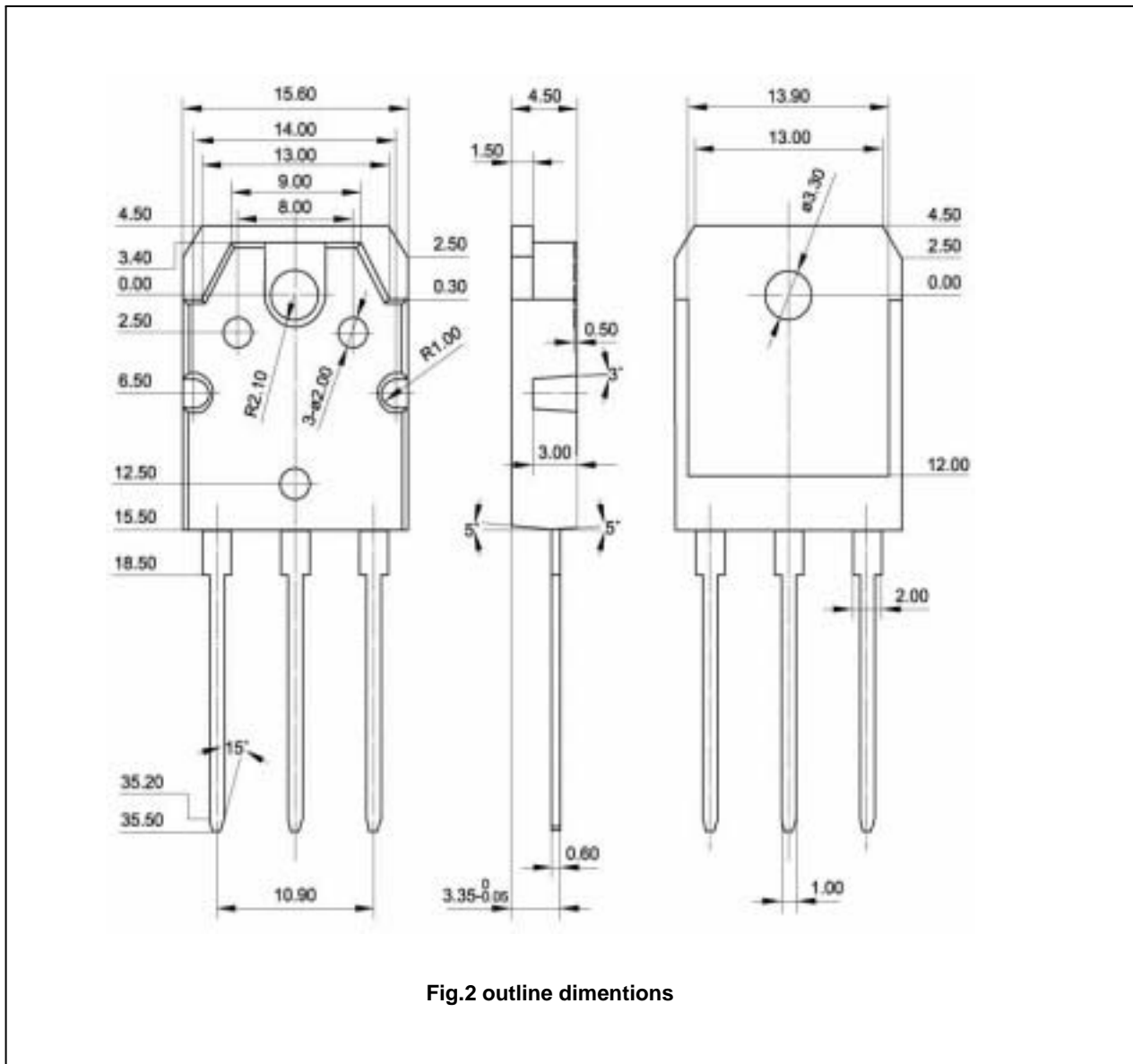


Fig.2 outline dimintions