Signetics

TDA8432

Computer-Controlled Deflection Processor for Video Displays

Objective Specification

Linear Products

DESCRIPTION

The TDA8432 is an I^2C bus-controlled deflection processor (analog picture geometry processor) which contains the control and drive functions of the deflection circuits in a computer-controlled TV (CCTV) or monitor. This IC replaces all picture geometry settings which are performed manually during manufacturing. The alignment of 10 picture geometry parameters for the vertical and horizontal deflection is accomplished by means of a microcontroller via the I^2C bus. Furthermore, it eliminates the external components needed for adjusting the horizontal frequency and phase position, vertical linearity, picture height, east-west parabola, and picture width. The east-west shaping circuit is also eliminated. Provisions have been incorporated to make several sync processor (TDA2579 and TDA2595) functions I^2C bus-controllable.

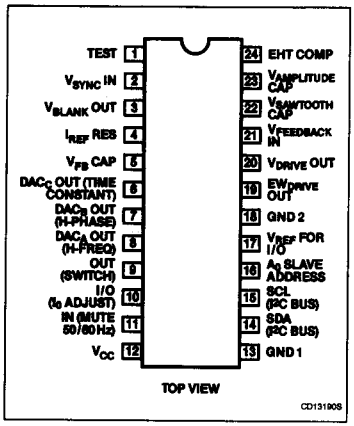
FEATURES

- **I^2C bus interface for all functions**
- **Input for vertical sync from sync processor**
- **Vertical sawtooth generator with frequency-independent amplitude**
- **Vertical output stage with feedback input for driving a vertical deflection amplifier**
- **East-west raster correction drive output**
- **EHT modulation input, providing optimum picture geometry compensation for static and dynamic EHT load variations**
- **I^2C bus-controlled alignment of 10 deflection parameters**
- **Provisions for controlling a sync processing IC which does not have an I^2C bus interface, including:**
  - **Two digital-to-analog converters for alignment of the free-running horizontal frequency and horizontal phase position**
  - **An I/O pin enabling computer alignment of the free-running horizontal frequency**
  - **A special purpose 4-level output for time constant switching of the horizontal phase-locked loop**
  - **A special purpose 3-level input for detection of the mute function and the 50Hz/60Hz state of the sync processor**
- **A switchable output (e.g., for controlling a video source selector)**

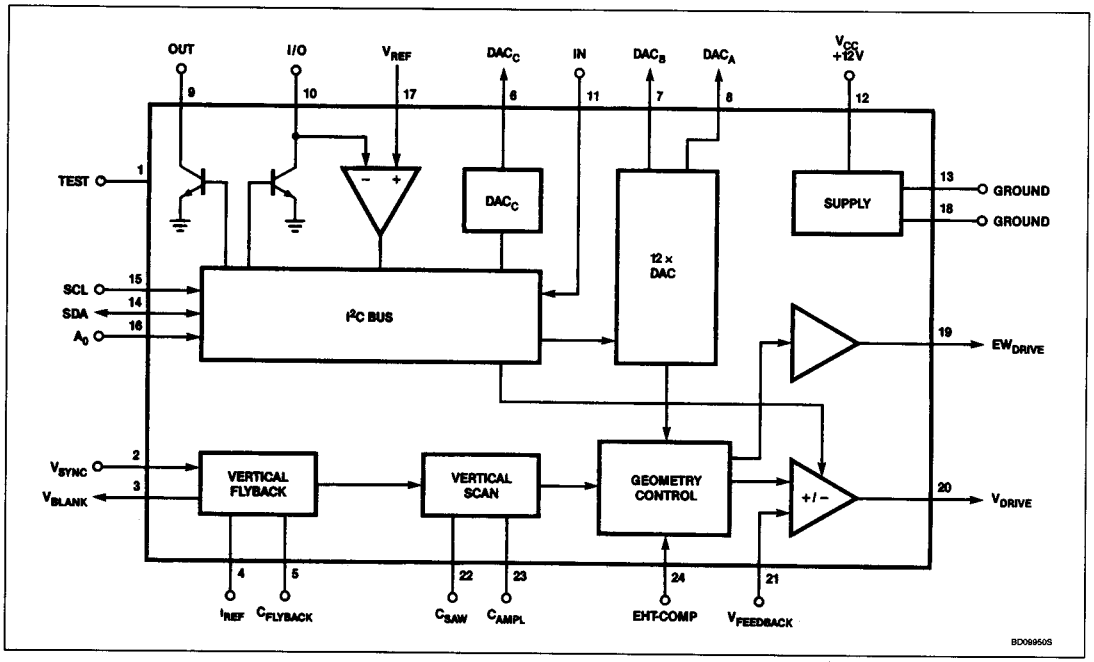
APPLICATIONS

- **Video monitors**
- **Color TV receivers**

PIN CONFIGURATION



BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (Pin 17)	14	V
	Switching voltage (Pin 5)	8	V
	Output currents of each pin to ground (Pins 11 and 12)	−10	mA
	Maximum short-circuit time outputs	10	sec
T_{STG}	Storage temperature	−55 to +150	°C
T_A	Operating temperature	−25 to 80	°C
T_J	Junction temperature	+150	°C
θ_{JA}	Thermal resistance	75	°C/W

RECOMMENDED OPERATING CONDITIONS In application circuit Figure 1 at $T_A = 25°C$ and $V_{CC} = 12V$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage (Pins 17 − 20, 10)	10		13.2	V
I_{CC}	Supply current (Pin 17)		42	55	mA
	Switching voltage VHF (Pin 5)	0		1.5	V
	Switching voltage hyperband	2		3.5	V
	Switching voltage UHF (Pin 5)	4		5	V
	Switching current UHF (Pin 15)			0.2	mA

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
VHF mixer including IF, measurement in circuit of Figure 1					
f_R	Frequency range: printed circuit board	50		300	MHz
	Noise Figure 1 (Pin 23) 50MHz 225MHz 300MHz		7.5 9 10	9 10 12	dB dB dB
	Optimum source admittance (Pin 23) 50MHz 225MHz 300MHz		0.5 1.1 1.2		mmho mmho mmho
	Input conductance (Pin 23) 50MHz 225MHz 300MHz		0.23 0.5 0.67		mmho mmho mmho
C_{IN}	Input capacitance (Pin 23) 50MHz − 300MHz		2		pF
V_{IN}	Input voltage for 1% × mod in channel (Pin 23)	97	100		dBμV
V_{IN}	Input voltage for 10kHz pulling (in channel) (Pin 23)	100	108		dBμV
A_V	Voltage gain = 20log (V_{11-12}/V_{23}) (Pins 11 − 12, 23)	22	24.5	27	dB
VHF mixer					
	Conversion transadmittance mixer = SC = I15/V23 = −I16/V23 (Pins 15, 16 − 23)		3.8		mmho
	Output admittance mixer (Pins 15 − 16)		0.1		mmho
	Output capacitance mixer (Pins 15 − 16)		2		pF

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
VHF oscillator					
f_R	Frequency range	70		330	MHz
	Shift V_B = 10%; 70 to 330MHz			200	kHz
	Drift T = 15°; 70 to 330MHz			250	kHz
	Drift from 5 seconds to 15 minutes after switching on			200	kHz
Hyperband mixer including IF (measured in circuit of Figure 1[2]) (measurements with hybrid)					
f_R	Frequency range	300		470	MHz
	Noise figure (Pins 21, 22) 300MHz 470MHz		8 8	10 10	dB dB
	Input reflection coefficient (Pins 21, 22) 300MHz $\|S11\|^5$ phase 470MHz $\|S11\|$ phase		−4.4 +162 −4.7 +151		dB deg dB deg
	Input available power Pav for 1% X-mod 300MHz in-channel (Pins 21, 22) 470MHz		−19 −19		dBm dBm
	10kHz pulling (in-channel) (Pins 21, 22) 470MHz N + 5 − 1MHz pulling[3] (Pins 21, 22) 470MHz		−11 −29		dBm dBm
	Gain = [4] 300MHz 470MHz	34 34	37 37	40 40	dB dB
Hyperband oscillator					
	Frequency range (MHz)	330		520	MHz
	Shift ΔV_B = 5%			400	kHz
	Drift ΔT = 15°			500	kHz
	Drift from 5 seconds to 15 minutes after switching on			600	kHz
	Input reflection coefficient (Pins 4 − 5) $\|S11\|$ at f = 330MHz phase		TBD TBD		dB deg
UHF mixer including IF (Pins 18 and 19) (measured in circuit of Figure 1[2]) (measurements with hybrid)					
	Frequency range	470		860	MHz
	Noise figure 470MHz 860MHz		8 9	10 11	dB dB
	Input reflection coefficient 470MHz $\|S11\|$ phase 860MHz phase		−4 +157 −4.2 +138		 deg deg
	Input available power P_{AV} for 470MHz 1% X-mod in-channel 860MHz		−19 −19		dBm dBm
	10kHz pulling (in-channel) 860MHz N + 5 − 1MHz pulling[3] 820MHz	 −42	−10 −35		dBm dBm
	Gain = [4] 470MHz 860MHz	34 34	37 37	40 40	dB dB

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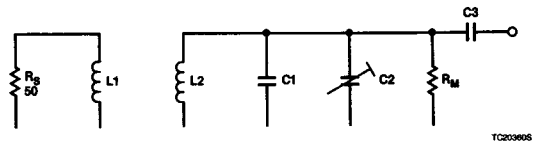
DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
UHF oscillator					
f_R	Frequency range (MHz)	500		900	MHz
	Shift $\Delta V_B = 5\%$			400	kHz
	Drift $\Delta T = 25°C$ to $40°C$			500	kHz
	Drift from 5 seconds to 15 minutes after switching on			300	kHz
IF amplifier					
			Mod	**Phase**	
	S11 S21 S12 S22 — measured at 36MHz, differentially		−0.5 12 −41 −7.9	−1 160 −5.2 13.7	dB/deg dB/deg dB/deg dB/deg
LO output (Pin 2)					
	Output voltage into 75Ω f ≤ 330MHz	14	37	100	mV
	Output reflection coefficient (VHF position) S22 (Hyperband and UHF) at 500MHz		TBD TBD		dB/deg dB/deg
	Spurious signal on LO output wrt LO output signal, measured in 75Ω with RF signal level at Pin 24 1V ≤ 225MHz 0.3V 225MHz – 300MHz			−10	dB
	Harmonics of LO signal wrt LO signal, measured in 75Ω			−10	dB

NOTES:
1. The Pins 2, 5, 11, 12, 13, 14 withstand the ESD test.
2. Measured with an input circuit for optimum noise figure.
3. The values have been corrected for hybrid and cable losses. The symmetrical output impendance of the hybrid is 100Ω.
4. The input level of an N + 5 – 1MHz signal which is just visible (Amtsblatt 69).
5. The gain is defined as the transducer gain measured in Figure 1 + the voltage transformation ratio of L6-L7. The ratio is 6:1 (16dB).
6. All S parameters are referred to a 50Ω system.



NOTES:
Component values: F = 50MHz F = 225MHz F = 300MHz
L1 = L2 =
C1 =
C2 =
C3 =
R_M =

Electrical parameters of the circuit are (for appropriate impedance and selectivity)
Insertion loss
VSWR without IC
VSWR with IC
Impedance of tuned circuit without IC at VSWR = 1
Image suppression
Output impedance (source for IC)

Figure 1