FAIRCHILD SEMICONDUCTOR®

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MM74HC4040
12-Stage Binary Counter

Features

- Typical propagation delay: 16ns
- Wide operating voltage range: 2–6V
- Low input current: 1µA Max.
- Low quiescent current: 80µA Max. (74HC Series)
- Output drive capability: 10 LS-TTL loads

General Description

The MM74HC4040 is a high speed binary ripple carry counter. This counter is implemented utilizing advanced silicon-gate CMOS technology to achieve speed performance similar to LS-TTL logic while retaining the low power and high noise immunity of CMOS.

The MM74HC4040 is a 12-stage counter. This device is incremented on the falling edge (negative transition) of the input clock, and all their outputs are reset to a low level by applying a logical high on their reset input.

This device is pin equivalent to the CD4040. All inputs are protected from damage due to static discharge by protection diodes to V_{CC} and ground.

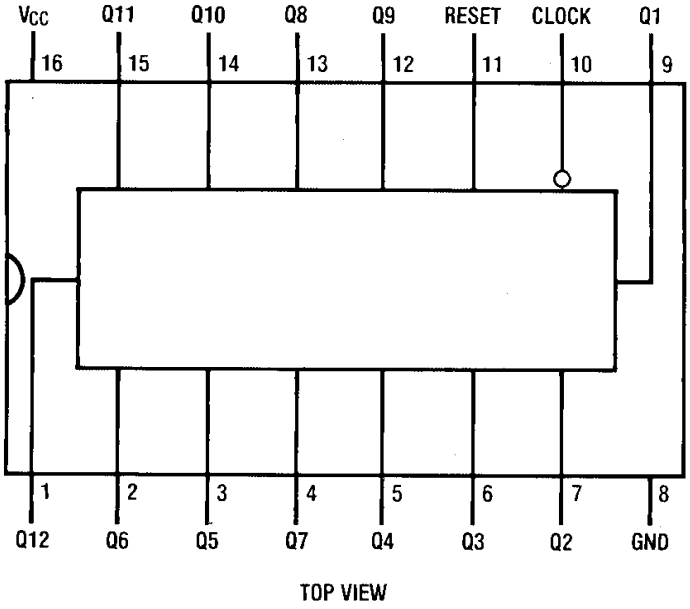
Ordering Information

Order Number	Package Number	Package Description
MM74HC4040M(1)	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC4040SJ(1)	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC4040MTC(1)	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC4040N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Note:

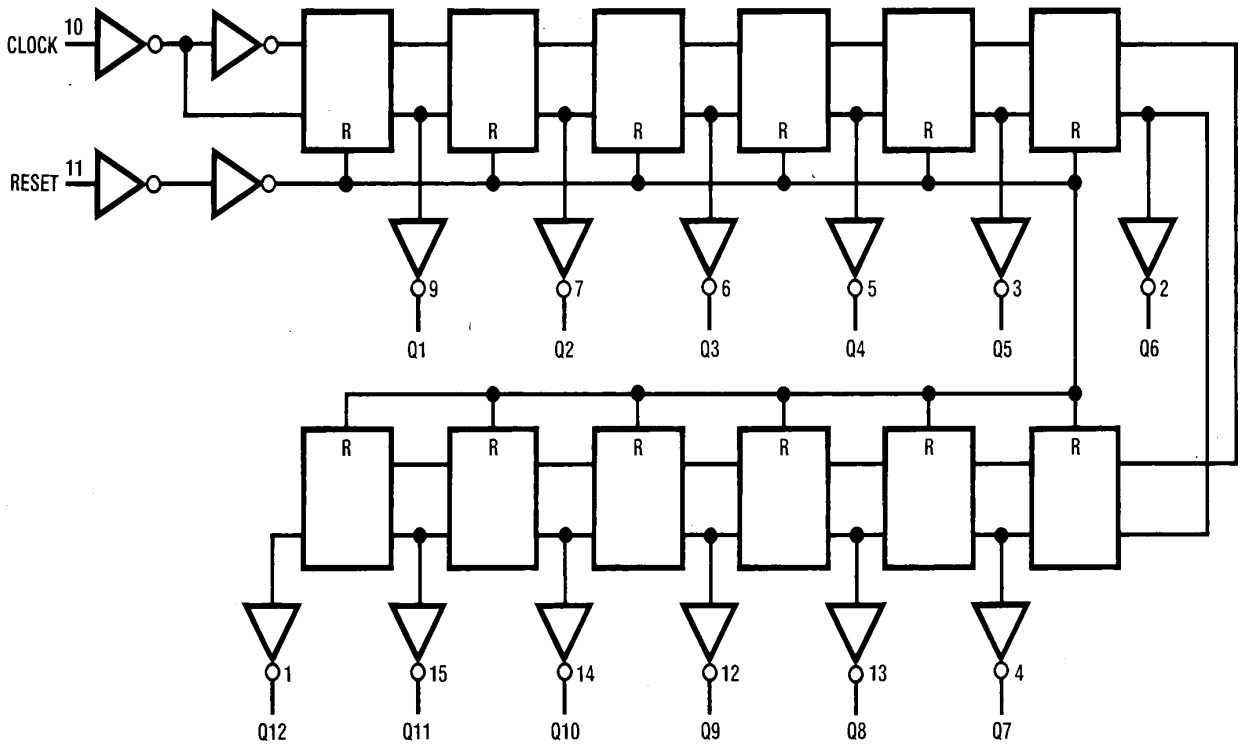
1. Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering number.

Connection Diagram



TOP VIEW

Logic Diagram



Absolute Maximum Ratings(2)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5 to +7.0V
V_{IN}	DC Input Voltage	–1.5 to V_{CC} +1.5V
V_{OUT}	DC Output Voltage	–0.5 to V_{CC} +0.5V
I_{CD}	Clamp Diode Current	±20mA
I_{OUT}	DC Output Current, per pin	±25mA
I_{CC}	DC V_{CC} or GND Current, per pin	±50mA
T_{STG}	Storage Temperature Range	–65°C to +150°C
P_D	Power Dissipation	
	Note 3	600mW
	S.O. Package only	500mW
T_L	Lead Temperature (Soldering 10 seconds)	260°C

Note:

2. Unless otherwise specified all voltages are referenced to ground.

3. Power Dissipation temperature derating — plastic “N” package: –12mW/°C from 65°C to 85°C.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	2	6	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	–40	+85	°C
t_r, t_f	Input Rise and Fall Times			
	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	
	V_{CC} = 6.0V		400	

DC Electrical Characteristics[4]

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	$T_A = -40$ to 85°C	$T_A = -55$ to 125°C	Units
				Typ.	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	
			6.0V		4.2	4.2	4.2	
V_{IL}	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	
			6.0V		1.8	1.8	1.8	
V_{OH}	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}: $\|I_{OUT}\| \le 20$ µA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	
			6.0V	6.0	5.9	5.9	5.9	
		$V_{IN} = V_{IH}$ or V_{IL}: $\|I_{OUT}\| \le 4.0$mA	4.5V	4.2	3.98	3.84	3.7	
		$\|I_{OUT}\| \le 5.2$mA	6.0V	5.7	5.48	5.34	5.2	
V_{OL}	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}: $\|I_{OUT}\| \le 20$ µA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	
			6.0V	0	0.1	0.1	0.1	
		$V_{IN} = V_{IH}$ or V_{IL}: $\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	.26	0.33	0.4	
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	.26	0.33	0.4	
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$µA	6.0V		8.0	80	160	µA

Note:

4. For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5$V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC} = 5$V, $T_A = 25°C$, $C_L = 15$pF, $t_r = t_f = 6$ns

Symbol	Parameter	Conditions	Typ.	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q	[5]	17	35	ns
t_{PHL}	Maximum Propagation Delay Reset to any Q		16	40	ns
t_{REM}	Minimum Reset Removal Time		10	20	ns
t_W	Minimum Pulse Width		10	16	ns

Note:

5. Typical Propagation delay time to any output can be calculated using: $t_P = 17 + 12(N–1)$ ns; where N is the number of the output, Q_W, at $V_{CC} = 5$V.

AC Electrical Characteristics

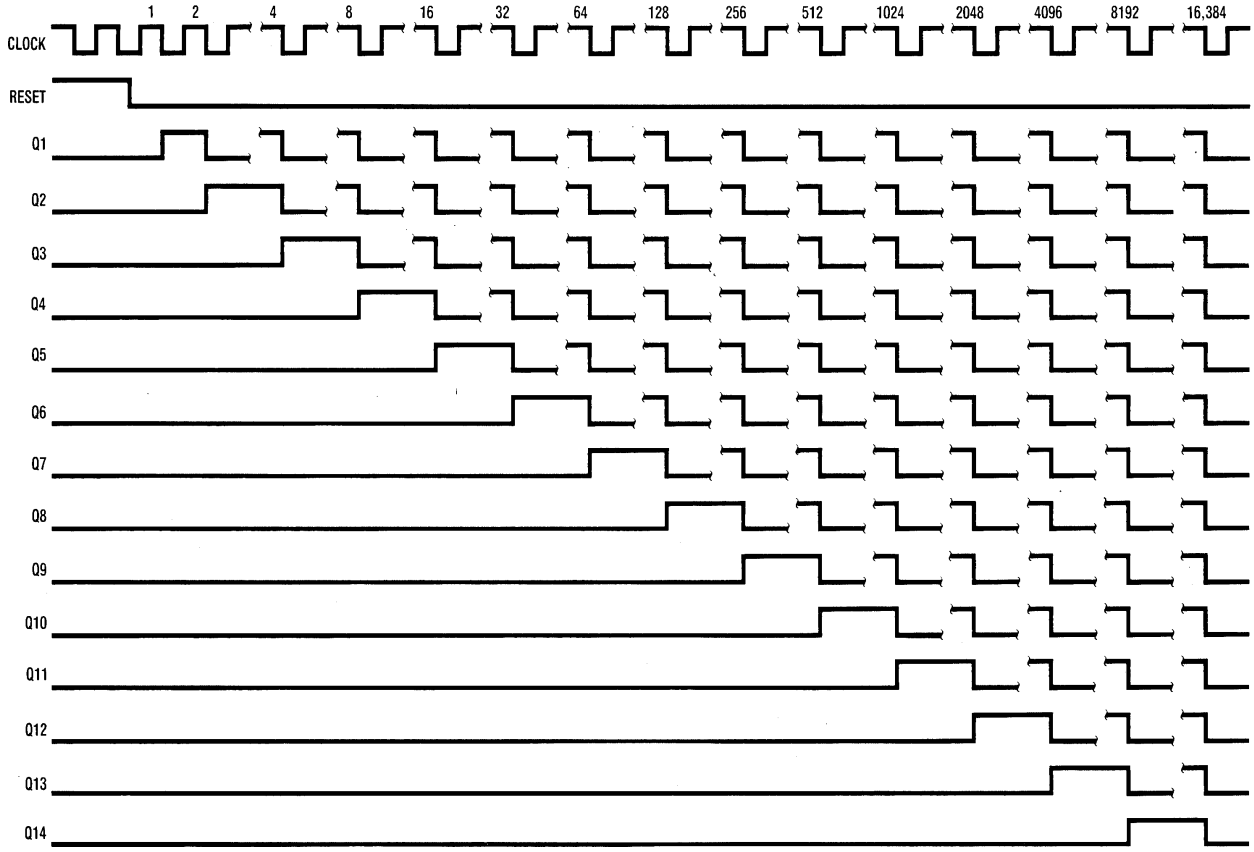
V_{CC} = 2.0V to 6.0V, C_L = 50pF, $t_r = t_f$ = 6ns (unless otherwise specified).

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	T_A = –40 to 85°C	T_A = –55 to 125°C		Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		2.0V	10	6	5	4	MHz
			4.5V	40	30	24	20	
			6.0V	50	35	28	24	
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q_1		2.0V	80	210	265	313	ns
			4.5V	21	42	53	63	
			6.0V	18	36	45	53	
t_{PHL}, t_{PLH}	Maximum Propagation Delay Between Stages from Q_n to Q_{n+1}		2.0V	80	125	156	188	ns
			4.5V	18	25	31	38	
			6.0V	15	21	26	31	
t_{PHL}	Maximum Propagation Delay Reset to any Q (4020 and 4040)		2.0V	72	240	302	358	ns
			4.5V	24	48	60	72	
			6.0V	20	41	51	61	
t_{REM}	Minimum Reset Removal Time		2.0V		100	126	149	ns
			4.5V		20	25	50	
			6.0V		16	21	25	
t_W	Minimum Pulse Width		2.0V		90	100	120	ns
			4.5V		16	20	24	
			6.0V		14	18	20	
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	
			6.0V	9	13	16	19	
t_r, t_f	Maximum Input Rise and Fall Time				1000	1000	1000	ns
					500	500	500	
					400	400	400	
C_{PD}	Power Dissipation Capacitance(6)	(per package)		55				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note:

6. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Timing Diagram



Physical Dimensions

Dimensions are in millimeters unless otherwise noted.

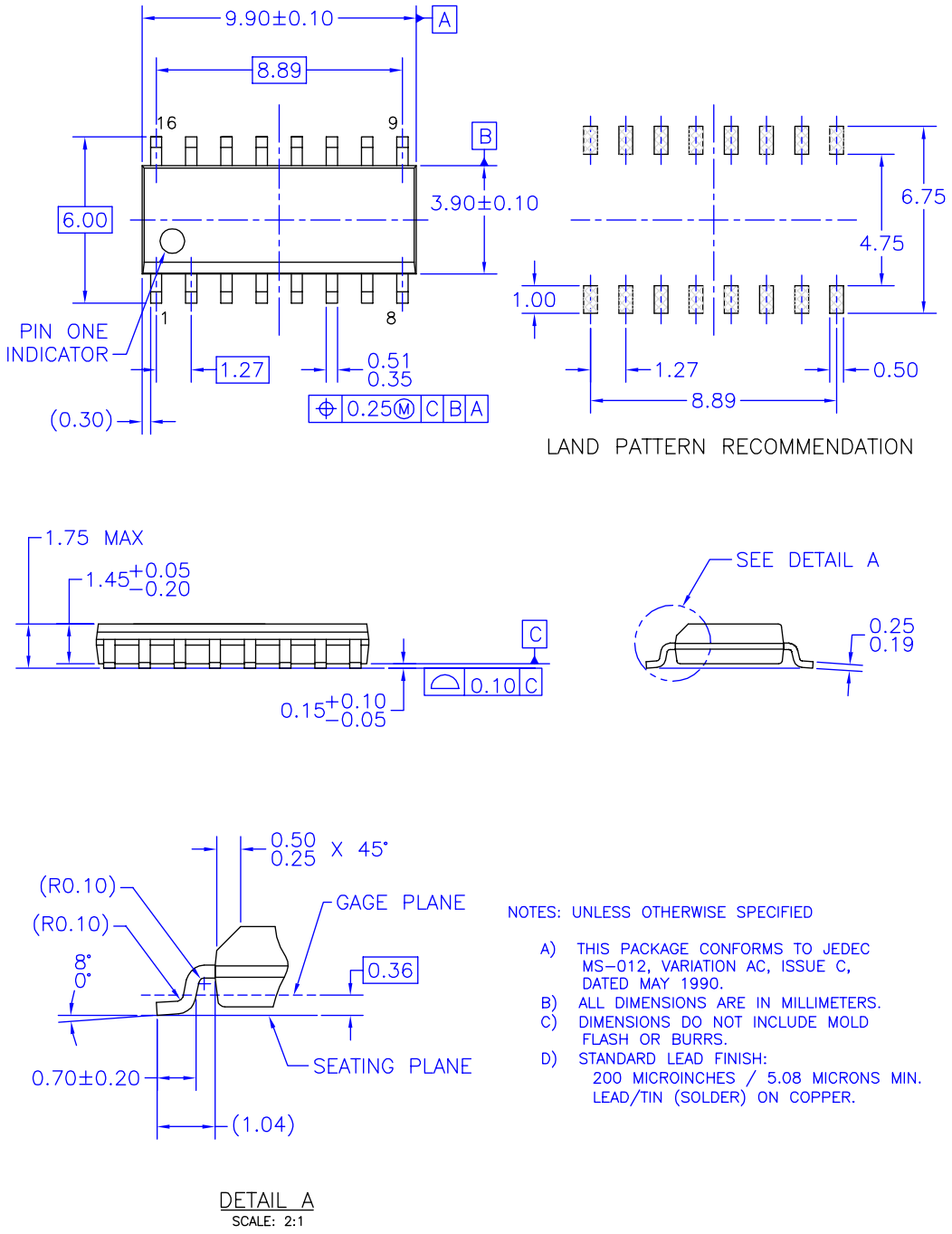
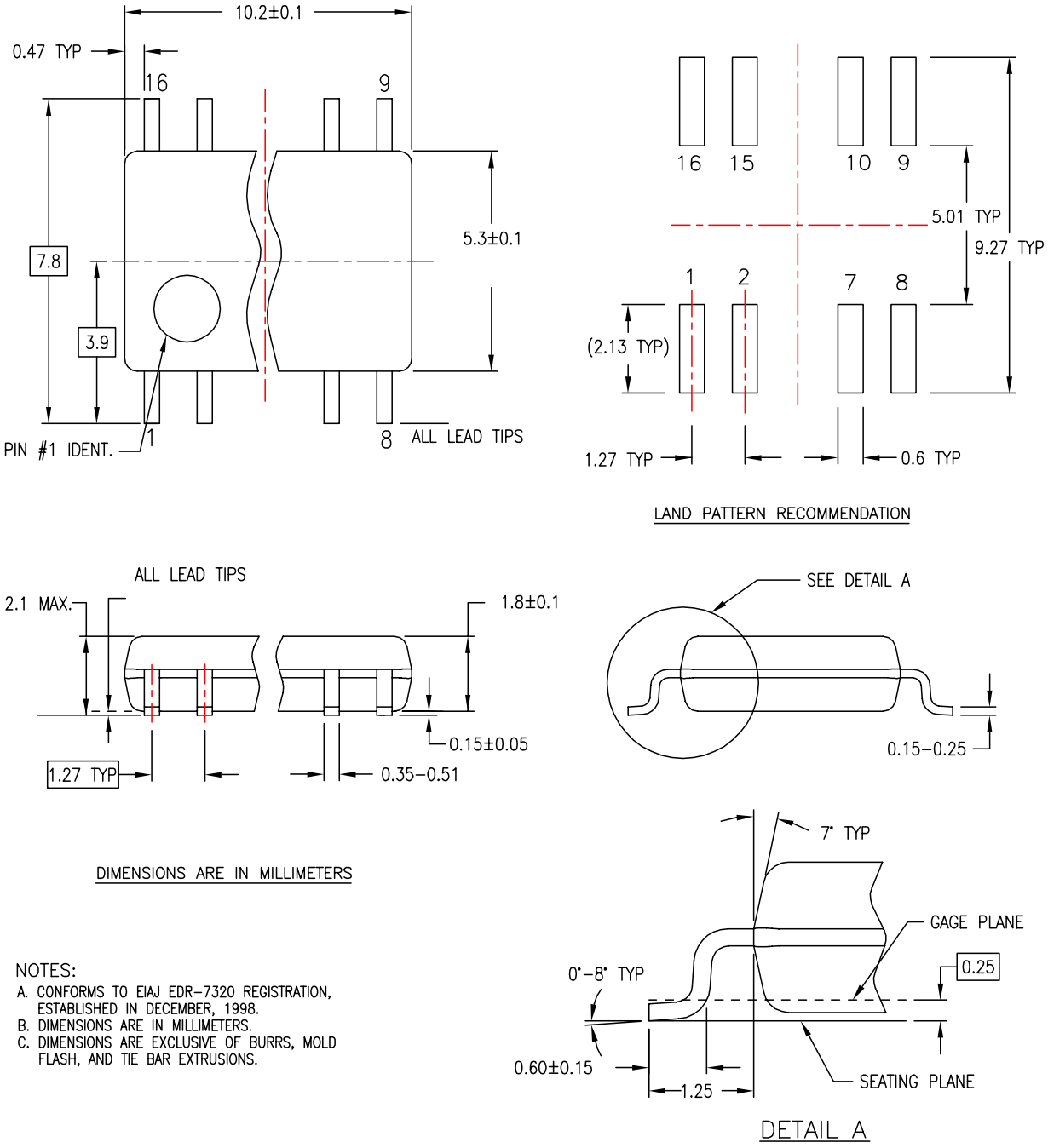


Figure 1. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

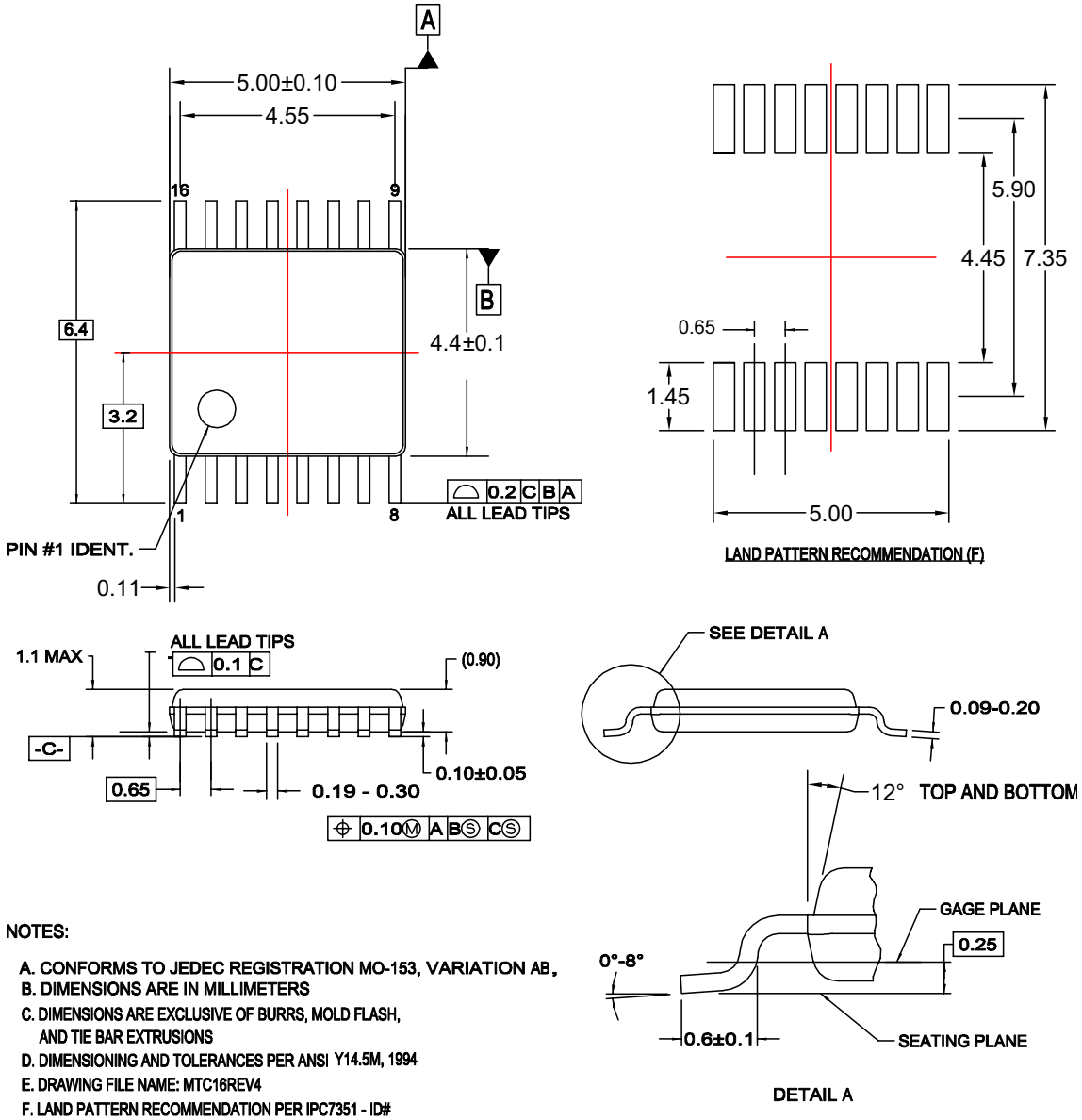
A. CONFORMS TO EIAJ EDR–7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DREVC

Figure 2. 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB,
B. DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1994
E. DRAWING FILE NAME: MTC16REV4
F. LAND PATTERN RECOMMENDATION PER IPC7351 - ID# TSOP65P640X110-16N

MTC16rev4

Figure 3. 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

Physical Dimensions (Continued)

Dimensions are in inches (millimeters) unless otherwise noted.

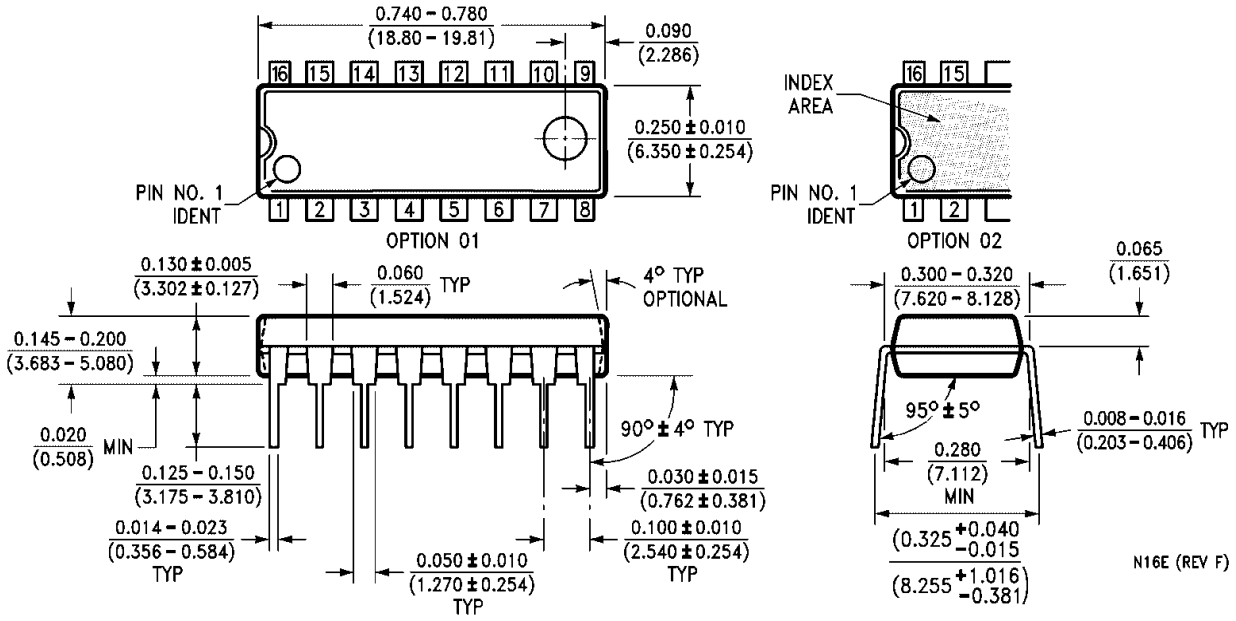


Figure 4. 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

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